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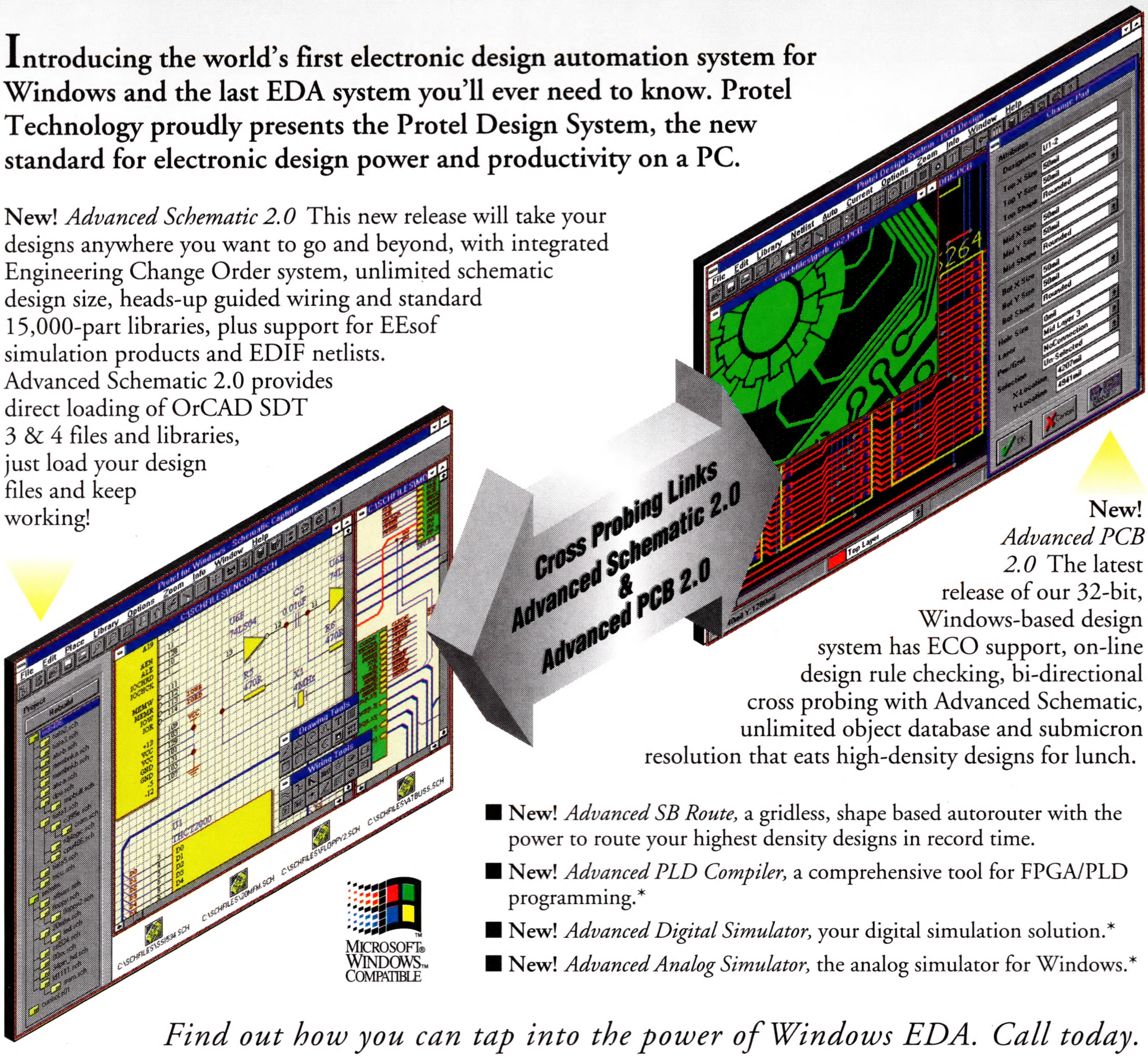

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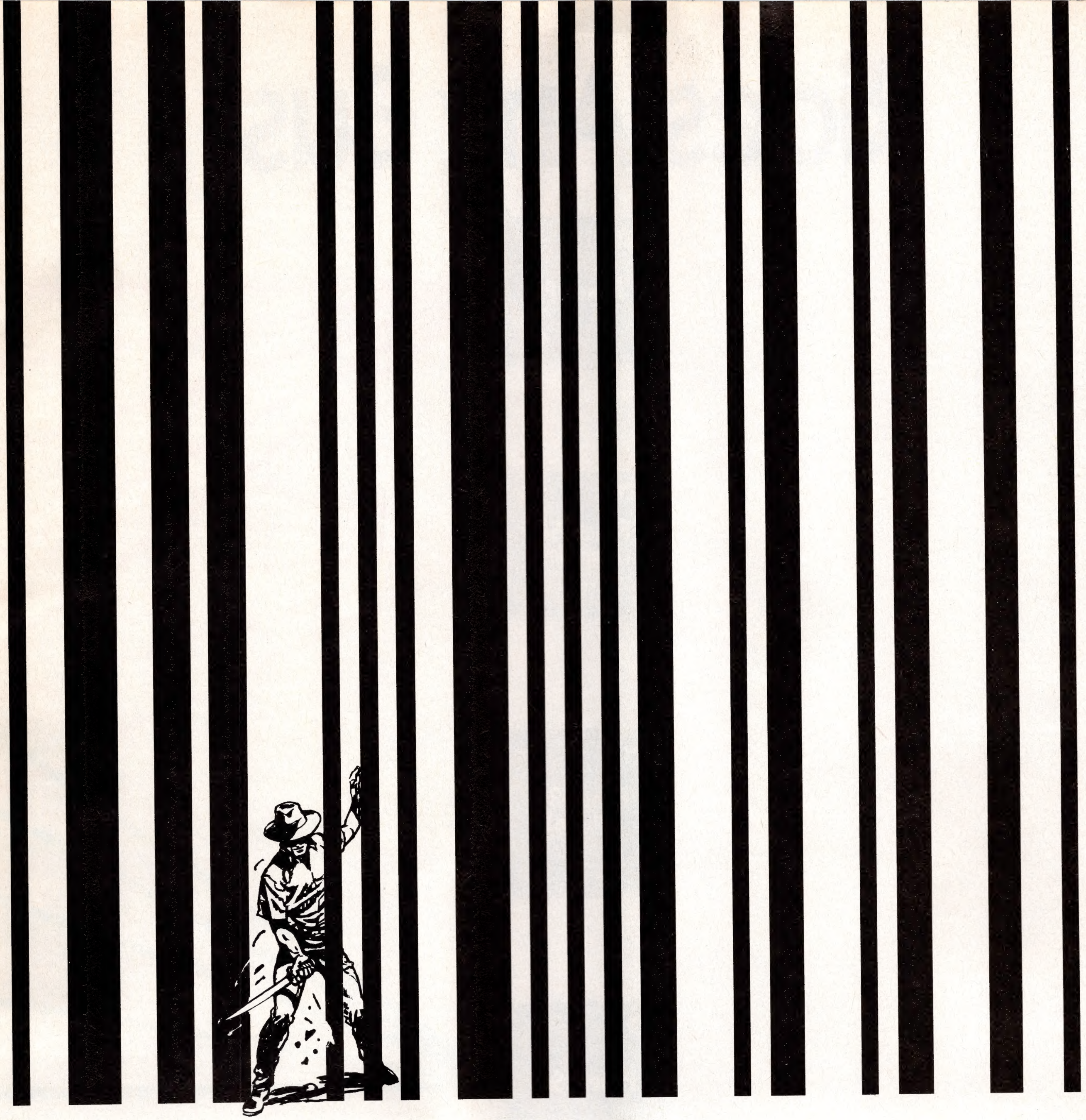

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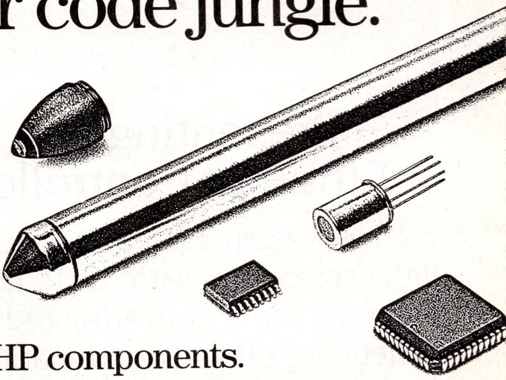

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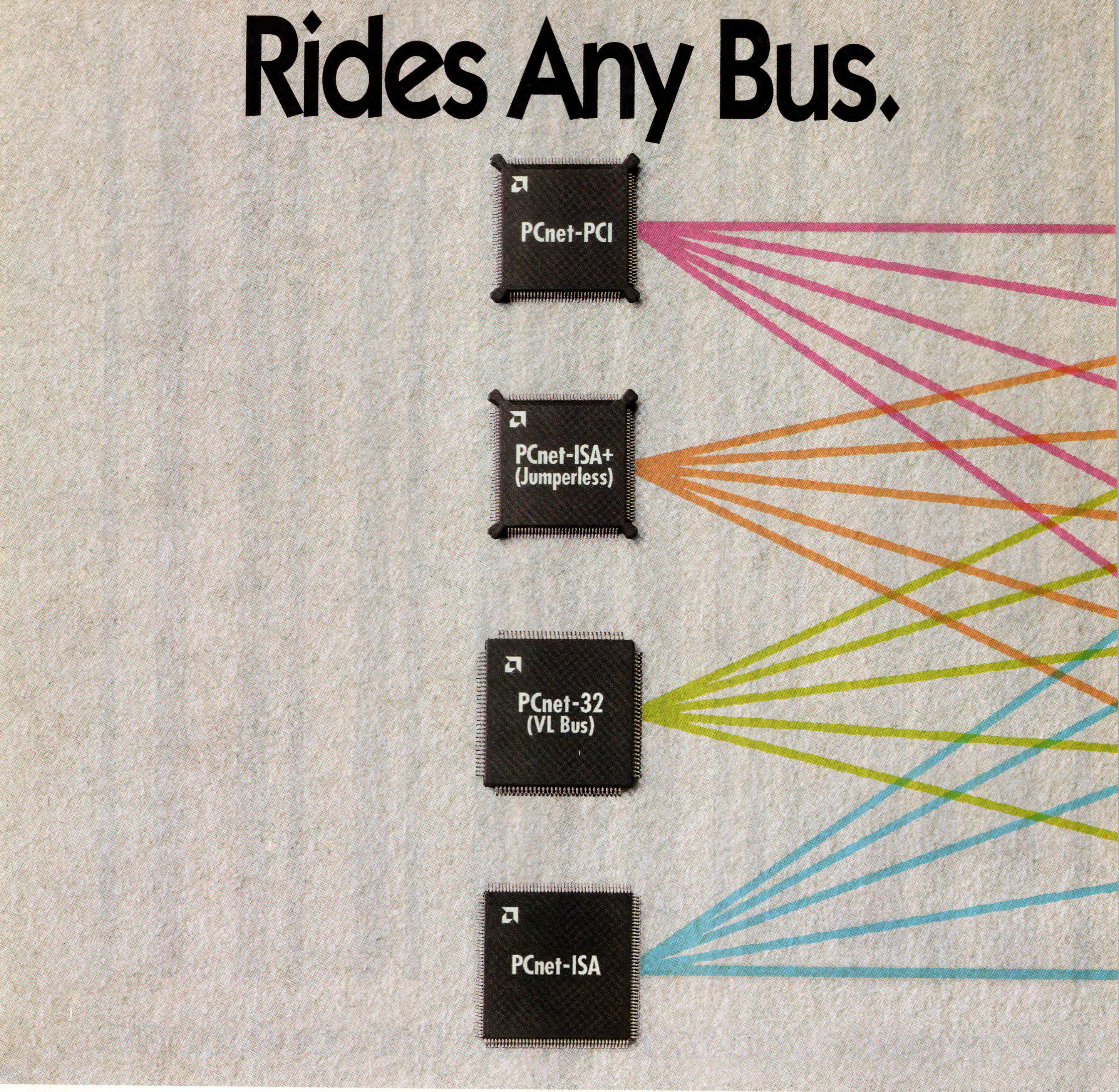

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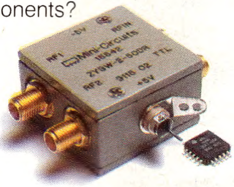

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RF Input (max dBm)	——	20	——	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
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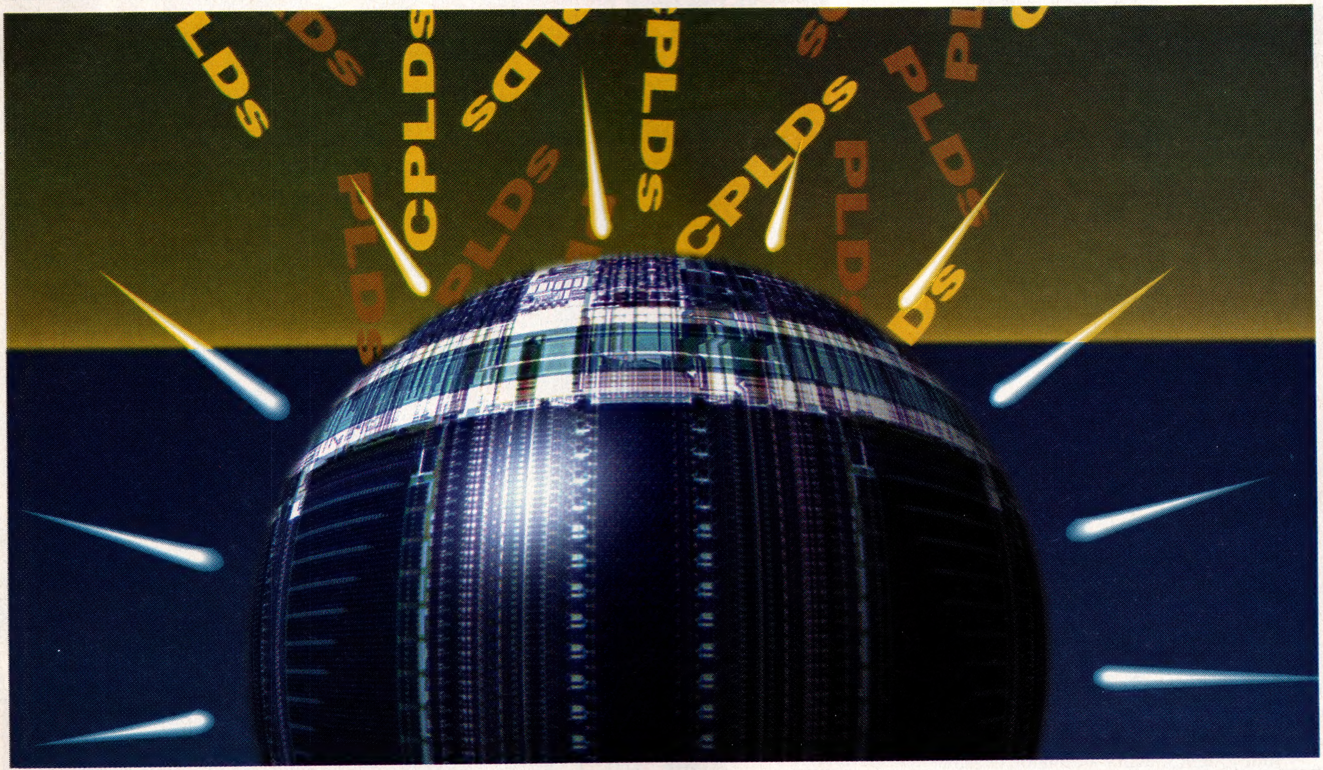

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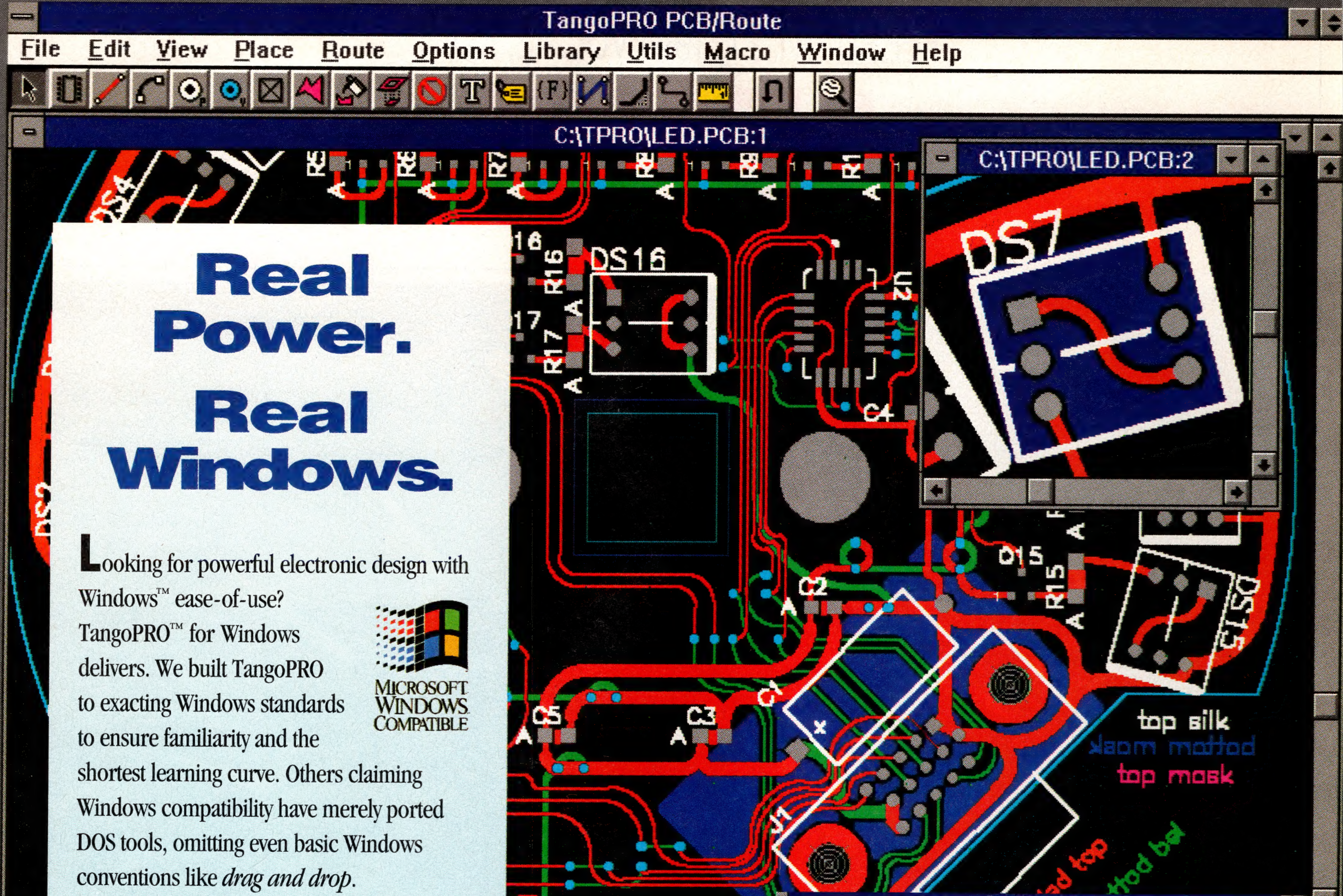

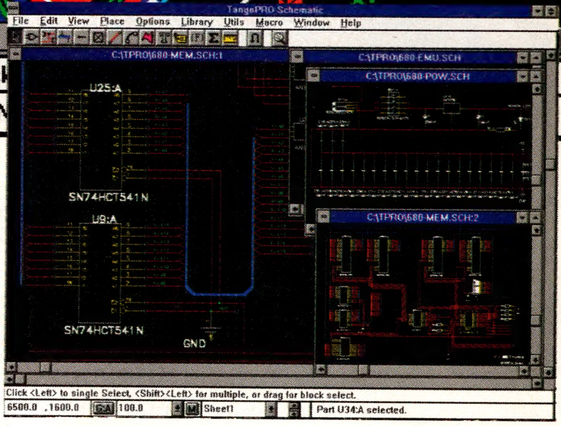

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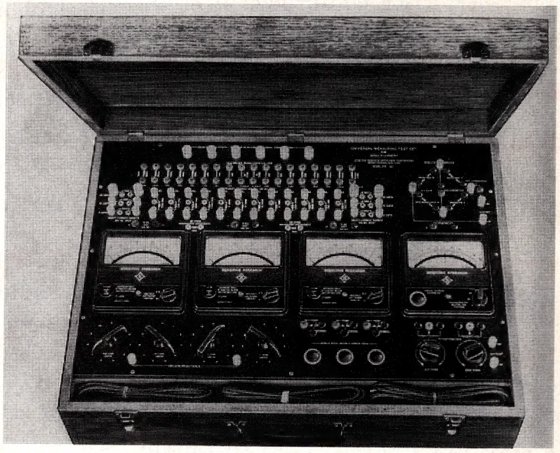

Three of the instruments are identical, each having a basic full scale sensitivity of 5ma, 20 ohms, 100mv; a 4” mirror scale; and an accuracy of 0.5%. These units provide a total of 96 ranges from 5ma full scale (lowest reading 50μamp) to 60 amp; and 100mv full scale (lowest reading 1mV) to 600v. They have a manually operated “key protection” which helps to guard the meters against overloads. The fourth instrument is a 5-range galvanometer with a basic sensitivity of 50-0-50μamp, and multiplying factors of 1, 3, 10, 30, and 100 to cover a wide range of galvanometer and microammeter ranges.

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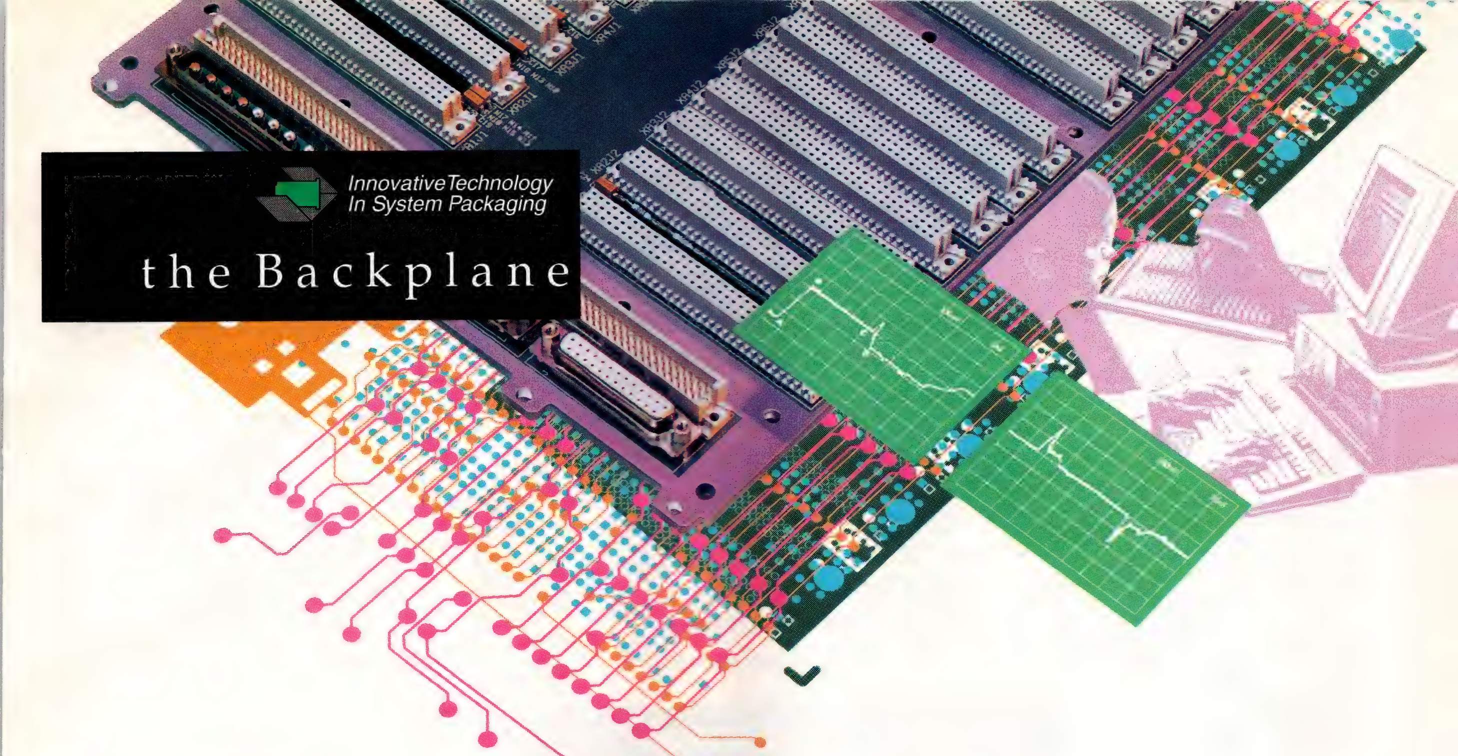
There's nothing like a “substantial oak case” to give an instrument the feel of calibration-lab quality.—SS

Meetings: IRE-AIEE Conference on Transistor Circuits, Feb. 18-19.

Museum of the University of Pennsylvania. The program will reflect the present state of research and development in the transistor circuit field and will be geared to engineers already familiar with transistor operation. Reservations should be made through L. H. Good, RCA Victor Division, Bldg. 10-5, Camden, N.J.*(Electronic Design, February 1954, p. 16.)*

This is the announcement for what was essentially the first International Solid State Circuits Conference. The conference quickly became the premier venue to for describing advances in solid-state circuit design. Today, the ISSCC is still the leading international conference on new ICs, and each year ELECTRONIC DESIGN *devotes a considerable amount of editorial space to its many highlights. In this issue, a series of Special Reports comprehensively covers this year's conference.—SS*



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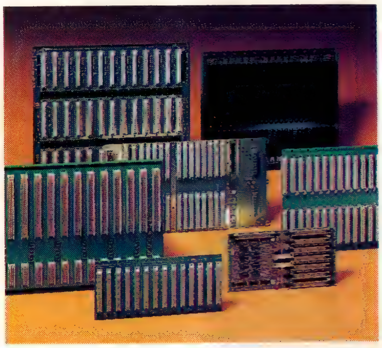

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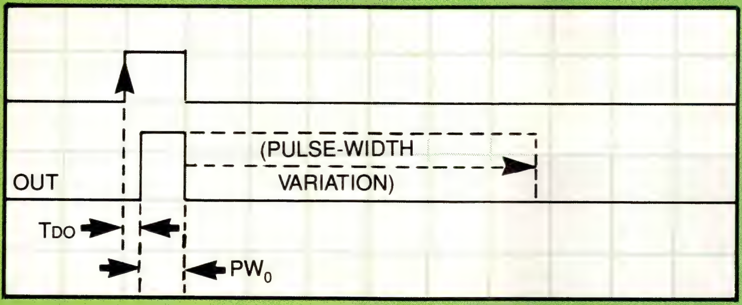

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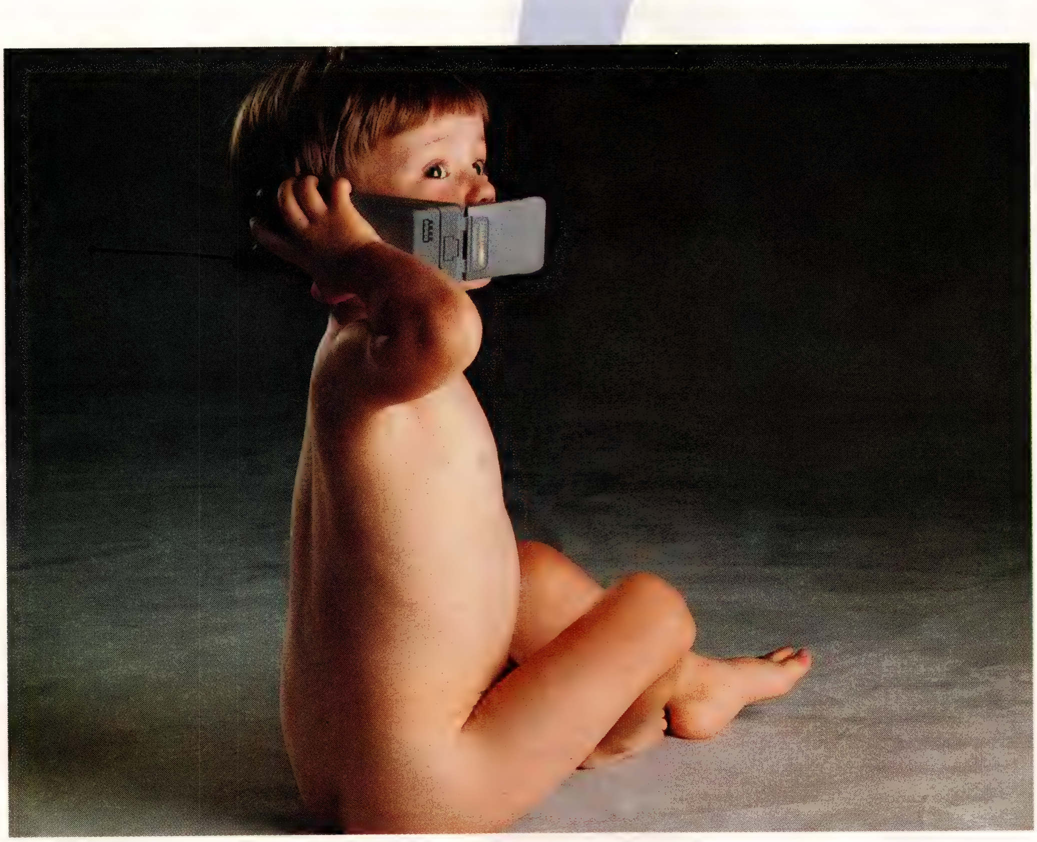

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UPCOMING MEETINGS

FEBRUARY

NEPCON West '94 Conference & Exposition, Feb. 27-Mar. 4. Anaheim Convention Center, Anaheim, CA. Contact NEPCON West '94, P.O. Box 552, Brookfield, IL 60513-0552; (708) 390-2420.

MARCH

IEEE COMPCON '94, Mar. 1-3. Stanford Court Hotel, San Francisco, CA. Contact Theodore Laliotis, HP Labs, 1501 Page Mill Rd., Palo Alto, CA 94304; (415) 857-8750; E-mail: Laliotis@hpl.hp.com.

1994 IEEE Symposium on Computer-Aided Control Systems Design (CACSD), Mar. 7-9. Tucson Convention Center, Tucson, AZ. Contact Professor Paul Battes, Engineering Professional Development, P.O. Box 9, Harvill Bldg., University of Arizona, Tucson, AZ 85721; (602) 621-5104.

mobile94 Conference & Exposition, Mar. 7-10. San Jose Convention Center, San Jose, CA. Contact Technologic Partners, 419 Park Ave. S., New York, NY 10016; (800) 326-3613.

International Verilog HDL Conference (IVC-94), Mar. 14-16. Westin Hotel, Santa Clara, CA. Contact Georgia Marszalek, 773 Widgeon St., Foster City, CA 94404; (415) 345-7477; fax (415) 341-0388.

CeBIT Hannover 94, Mar. 16-23. Hannover, Germany. Contact Sara Unger, Hannover Fairs USA, 103 Carnegie Ctr., Princeton, NJ 08540; (609) 987-1202; fax (609) 987-0092.

1994 20th Annual Northeast Bioengineering Conference, Mar. 17-18. Western New England College, Springfield, MA. Contact Dr. James V. Masi, Western New England College, Springfield, MA 01119; (413) 782-1344; fax (413) 782-1746.

1994 IEEE International Conference On Microelectronic Test Structures, Mar. 22-24. Catamaran Resort Hotel, San Diego, CA. Contact Ms. Sandra Grawet, All About Meetings, 2301 Artesia Blvd., Ste. 12-101, Redondo Beach, CA 90278; (310) 371-3438; fax (310) 371-1567.

1994 IEEE 6th International Conference on Indium Phosphide & Related Materials (IPRM), Mar. 28-31. Red Lion Resort, Santa Barbara, CA. Contact Ms. Susan Evans, IEEE/LEOS, 445 Hoes Ln., Box 1331, Piscataway, NJ 08855-1331; (908) 562-3896; fax (908) 562-1571.

1994 IEEE National Radar Conference, Mar. 29-31. Holiday Inn Crowne Plaza, Ravinia, Atlanta, GA. Contact Dr. Robert N. Trebits, Georgia Tech Research Inst., 7220 Richardson Rd., Smyrna, GA 30080; (404) 528-7769; fax (404) 528-7883.

SOUTHCON '94, Mar. 29-31. Orange County Convention/Civic Center, Orlando, FL. Contact Ms. JoAnn Lindberg, ECM, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668; fax (310) 641-5117.

APRIL

SOUTHEASTCON '94, April 10-13. Hyatt Regency Hotel, Miami, FL. Contact Dr. Osama A. Mohammed, Dept. of Electrical Eng., Florida Int'l University, University Park Campus, Miami, FL 33199; (305) 348-3040/3708; fax (305) 348-3707.

1994 IEEE International Reliability Physics Symposium, April 11-14. Fairmont Hotel, San Jose, CA. Contact Mr. Ajit Goel, Oneida Research Services, 540 Weddell Dr., Ste. 7, Sunnyvale, CA 94089; (408) 734-2982; fax (408) 734-2984.

1994 IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '94), April 19-22. Adelaide Convention Ctr., Adelaide, S. Australia. Contact Mr. Phil Plevin, Plevin & Assoc. Pty. Ltd., Box 54, Burnside 5066, S. Australia; (61) 8-379-8222; fax (61) 8-379-8177.

1994 IEEE 44th Electronic Components and Technology Conference (ECTC '94), April 30-May 5. Washington Hilton Hotel, Washington D.C. Contact Mr. James Bruorton, Kemet Electronics, P.O. Box 5928, Greenville, SC 29606; (803) 963-6621; fax (803) 963-6521.

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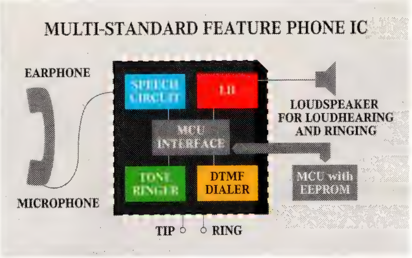

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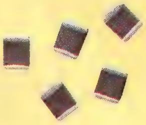
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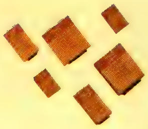
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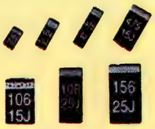
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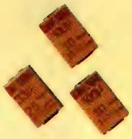
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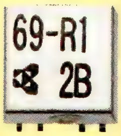

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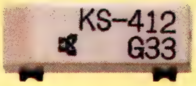

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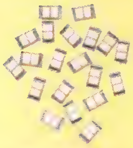
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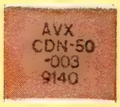

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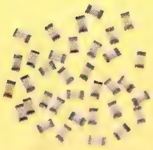
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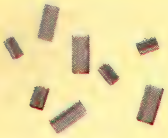
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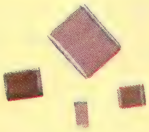
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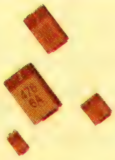
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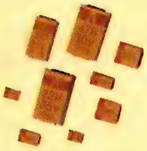
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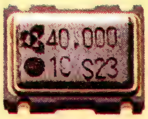

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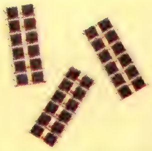
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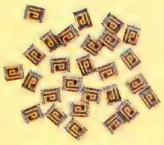
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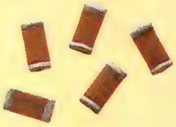
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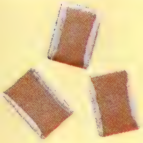
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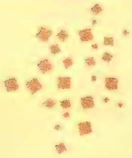
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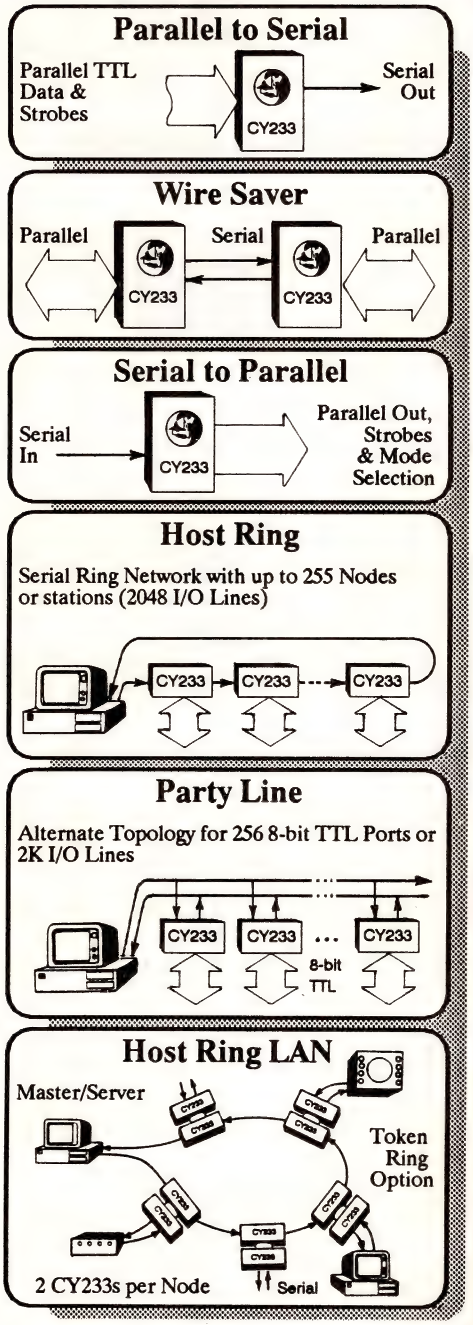

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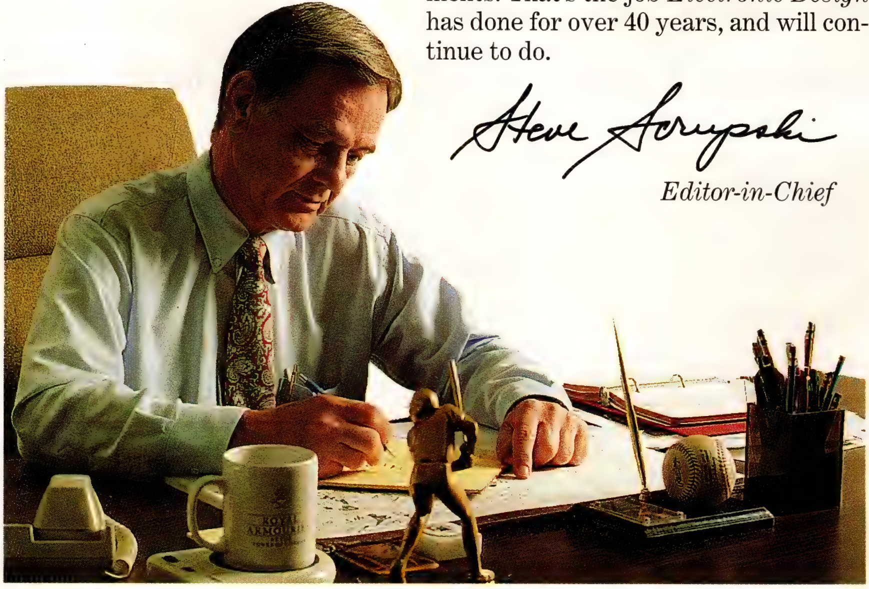
EDITORIAL

ONCE MORE, MUSINGS ON I-80 AT 5 MPH

I've often complained on this page about the traffic on Interstate Highway 80. I've also discussed how the mind tends to wander while I sit staring at a rear license plate and an exhaust pipe. What with the way the winter weather has been here in the Northeast, it seems that I could muse my way through a year's worth of these columns. Rather than subjecting the loyal readers of *Electronic Design* to such punishment, I'll settle for the following:

- In watching the turnaround in the U.S. automobile industry, it's difficult not to feel a great deal of satisfaction as a member of the electronics industry. To a large degree, the improvements in efficiency, reliability, and safety of U.S.-made autos can be attributed to the proliferation of electronics in various control systems. And what's even better, the demonstrated success of electronics in automotive applications will pay handsome dividends for the electronics industry. The average new auto now carries about $1200 worth of electronics, a figure that's growing by 15% a year, according to Hewlett-Packard.
- The business side of the electronics industry appears to be on a strong upswing nowadays. For instance, the semiconductor book-to-bill ratio continues to rise, good news about the 1994 outlook seems to arrive with every post, and consumers appear to have accepted, if not embraced, electronic aids. All in all, it appears that booming markets loom ahead in interactive digital TV, portable communications and computing devices, and electronics-rich automobiles, to name just a few.
- However, this enthusiasm for the industry's future business is tempered by a sense of unease regarding engineering employment. The continuing cutbacks in military and aerospace spending and the corresponding layoffs have rippled throughout the industry. Many engineers are being forced out of their profession because they happened to be in the wrong place, working on the wrong projects, and gaining experience in the wrong technologies—all at the wrong time. Somehow, they will have to refresh their skills, learn new technologies, and probably move to a new place if they're to remain a part of the industry.
- The electronics industry seems to re-invent itself every few years. Propelling the change, of course, is semiconductor technology: embedded microcontrollers refashioned automotive engine controls, 32-bit microprocessors are leading the way into image-processing, and dense DRAMs are handling memory-intensive applications in new desktop systems. Basically, semiconductor makers have opened up many new opportunities for the rest of the industry.

To keep ahead or at least stay on course within the industry's changing landscape, it's essential for top developers to stay abreast of breaking developments. That's the job *Electronic Design* has done for over 40 years, and will continue to do.



Steve Scrupski

Editor-in-Chief

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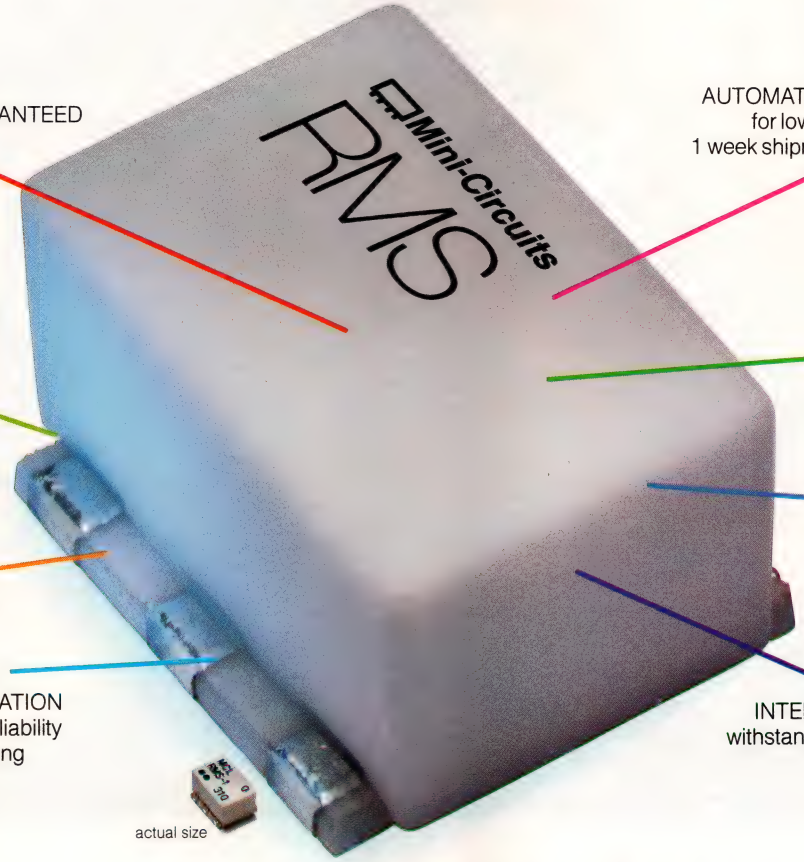

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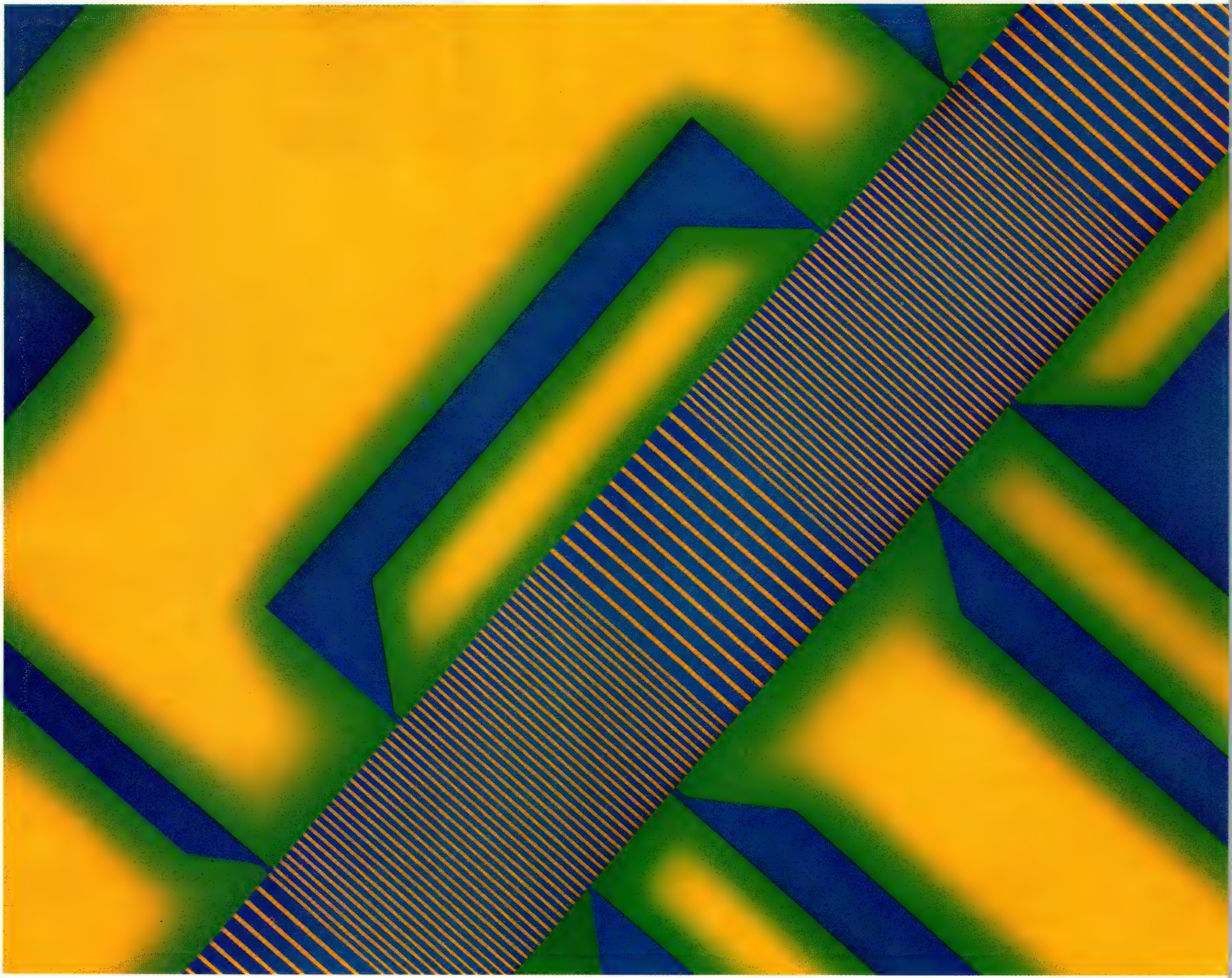

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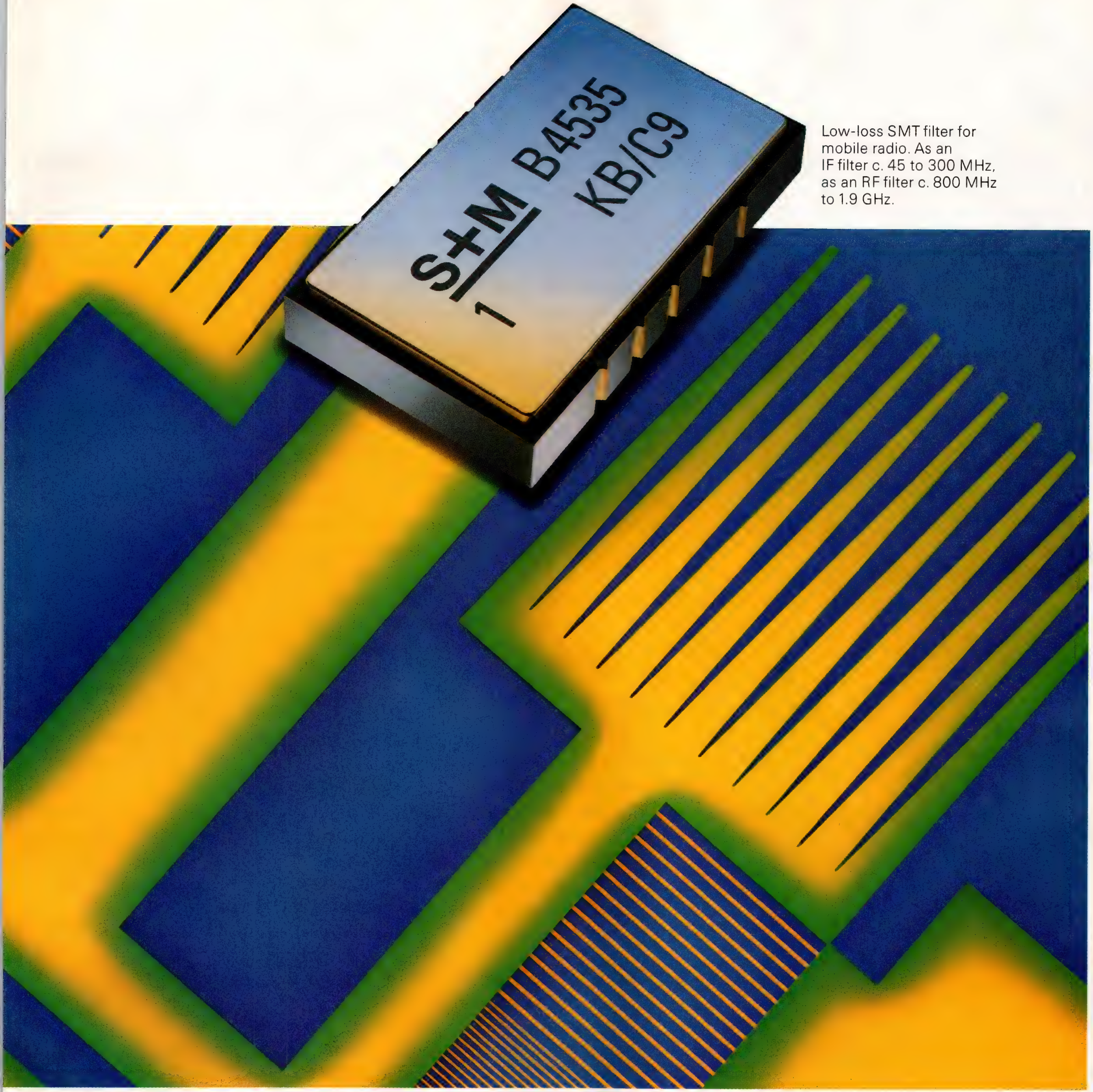

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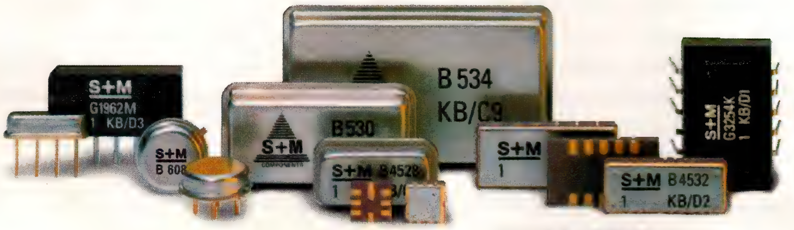

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PULLING OUT THE HARD-DISK DRIVE

The recent flood of notebook-sized computers coupled with the exorbitant storage requirements of popular operating systems and software applications are giving headaches to both system designers and hard-disk drive manufacturers. One remedy that's receiving increased attention is to design the system with the storage device as an external peripheral, using the PCMCIA-card form factor.

In a presentation delivered at *Electronic Design's* Portable By Design Conference (Feb. 14-18), Niteen Bhat of SunDisk Corp., Santa Clara, Calif., says that system designers should consider incorporating an interface that's compatible with the ATA (AT attachment) standard. By maintaining compatibility with the standard, users are free to obtain storage devices from a host of vendors, rather than being locked in to a particular vendor. In addition, the system vendor no longer needs to design in mass-storage devices (it also lets them lower the system price because there's no internal hard disk).

RICHARD NASS
COMPUTER SYSTEMS

The PC Card ATA standard is a combination of the ATA and PCMCIA standards and defines how solid-state mass-storage devices operate in a system with an ATA-compliant embedded design. As long as the embedded socket design complies with the PC Card ATA standard, system software changes aren't required when upgrading host systems. Moreover, the cards can be used in any system that's compatible with the standard. The standard also ensures backward compatibility, meaning that the card will also run in the next generation of compliant systems.

A register set and protocol along with a 40-pin connector are defined by the PC Card ATA standard. Relying on the electrical and mechanical characteristics of the AT bus, the standard can accommodate two daisy-chained drives. Mass-storage cards that comply have a built-in controller that makes the card appear to the host as if it were an ATA-compliant rotating disk.

Various hardware and software issues must be dealt with when designing a system utilizing PC Card ATA devices. On the hardware side, there are mechanical issues, power-supply considerations, and also the card-host interface. The mechanical concerns start with the physical size of the card: Should it fit the Type-1 (3.3 mm high), Type-2 (5 mm), or Type-3 (10.5 mm) form factor?

As for the interface, the issues involve interrupts, memory size and type, and socket-control conflicts. For instance, the card is required to use an 8- or 16-bit memory-mapped window with a polling mode. It also must support memory, contiguous I/O, and primary and secondary I/O modes.

The PCMCIA specification defines a layered software protocol for a standard software interface. The main layers are the card and socket services, and the client device drivers. Socket services allow higher-level software to control and access socket hardware through a predefined set of functions. The card services handle the client device drivers, operating systems, and application requests made to the card.

The card's software depends on its hardware, particularly the interface. Standard BIOS is available from various vendors. The same BIOS routine, tailored to the system's architecture, should operate with varying generations of systems, even spanning different media types, such as rotating or flash-memory disk drives. For non-DOS-based systems, system designers may have to develop their own device drivers. When developing a proprietary driver, designers must consider the sequence that occurs when the card is first inserted during the initialization process. The host system needs to detect when the card is inserted, determine the card type based on the card-services information, and configure the card or socket for the appropriate mode based on the available I/O and memory resources.

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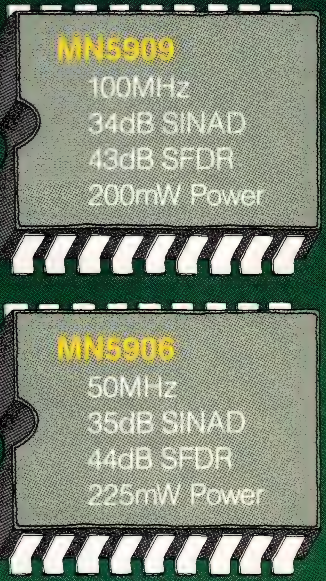

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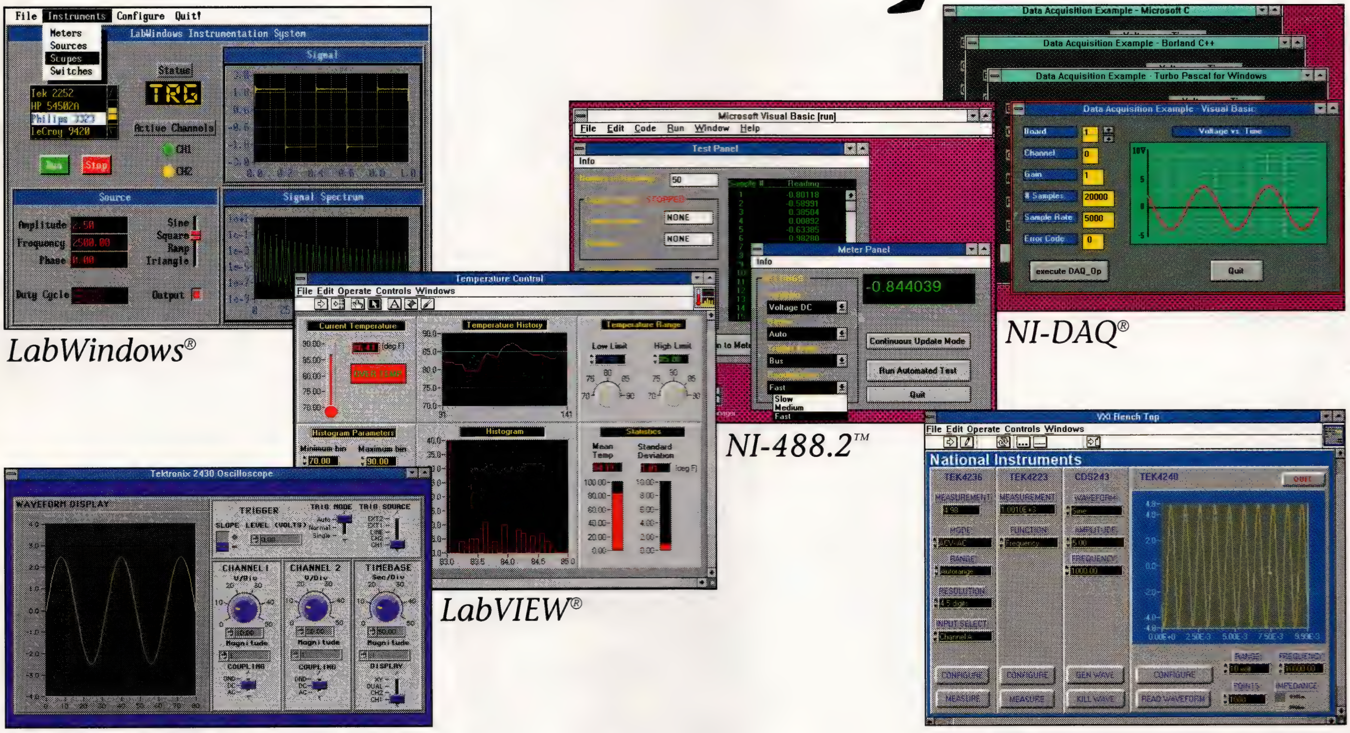
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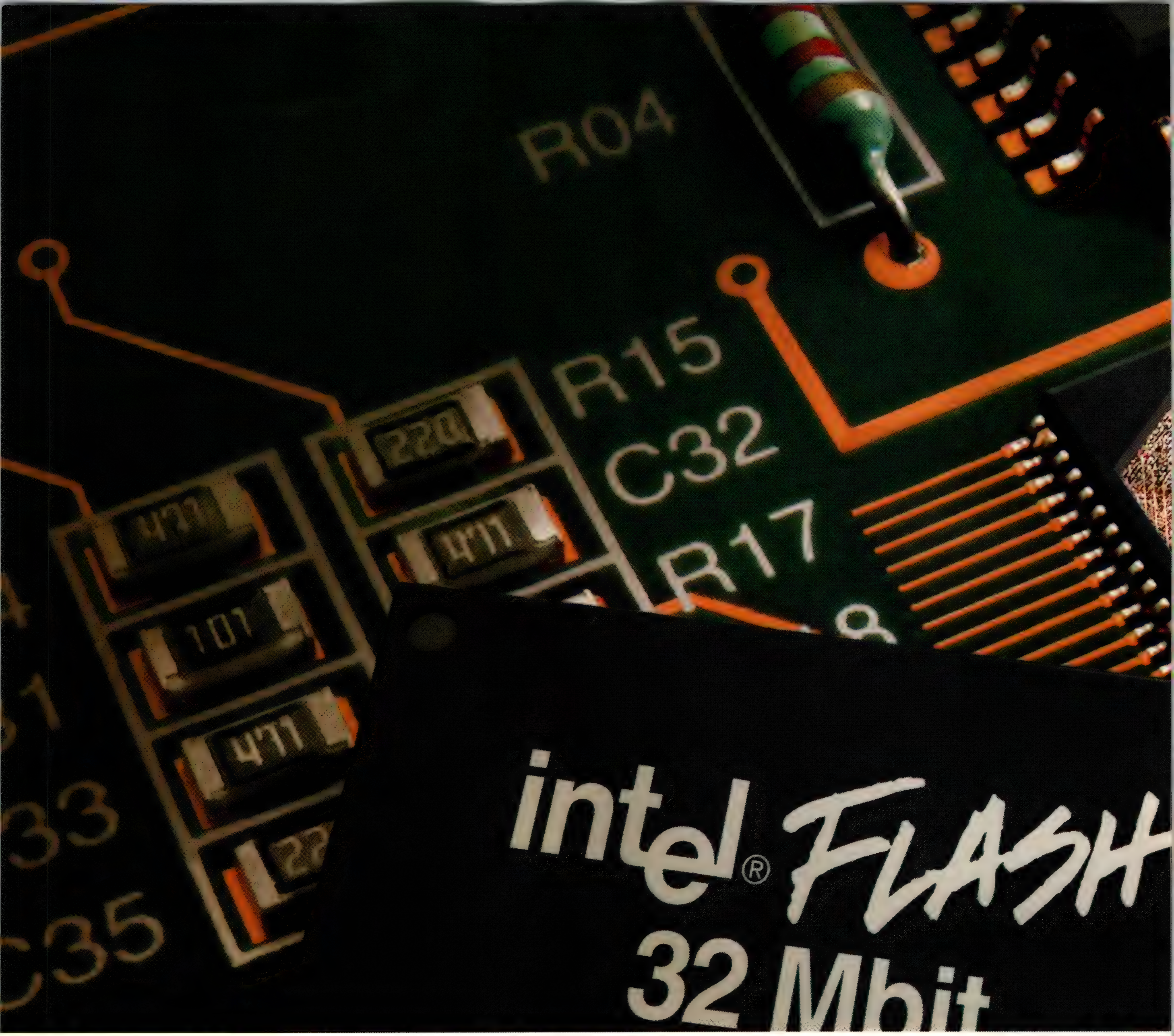

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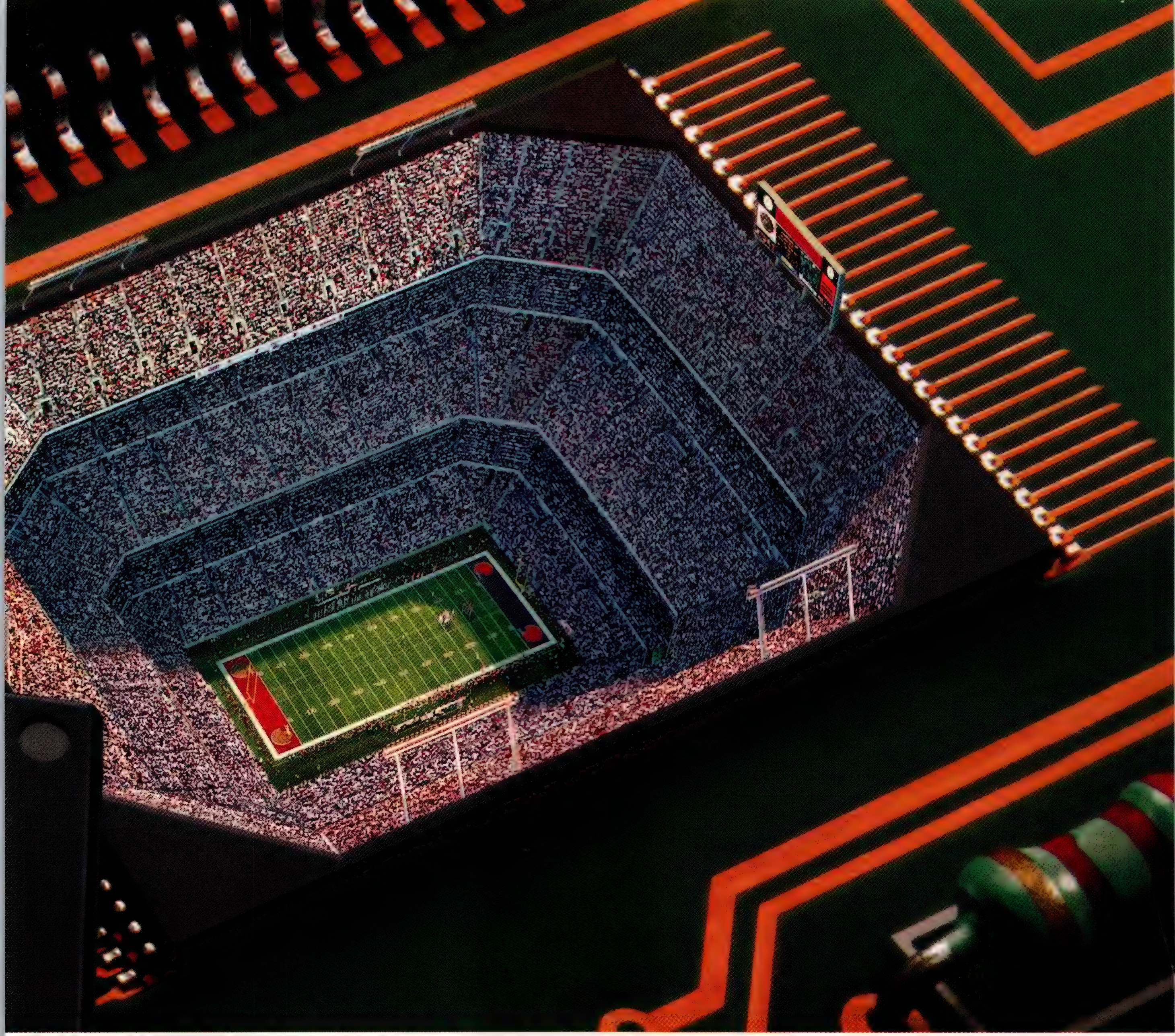

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Company-wide, the recycling spirit has spread from Cleveland headquarters to offices throughout the country. Penton employees are enthusiastic participants in expanding programs to re-use paper, aluminum cans, and other waste materials.

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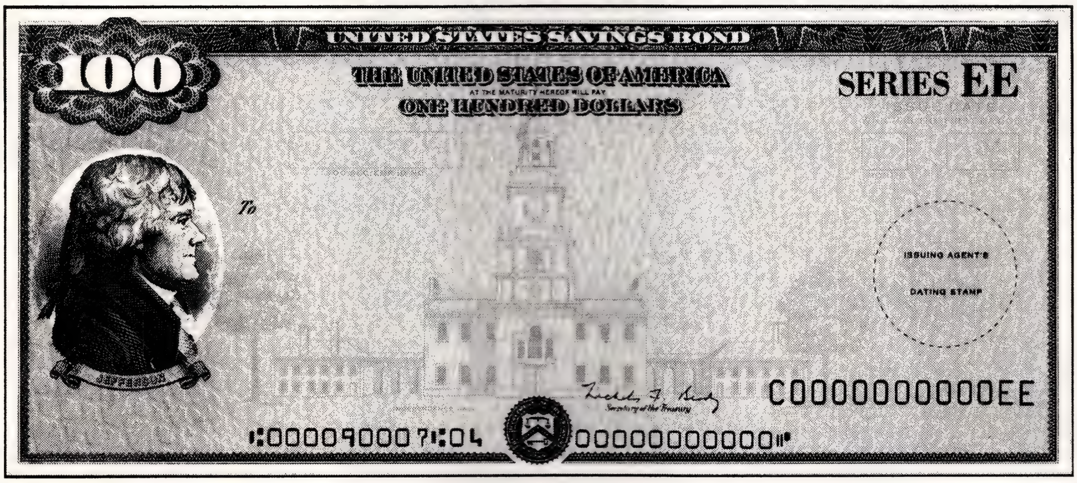
Penton Publishing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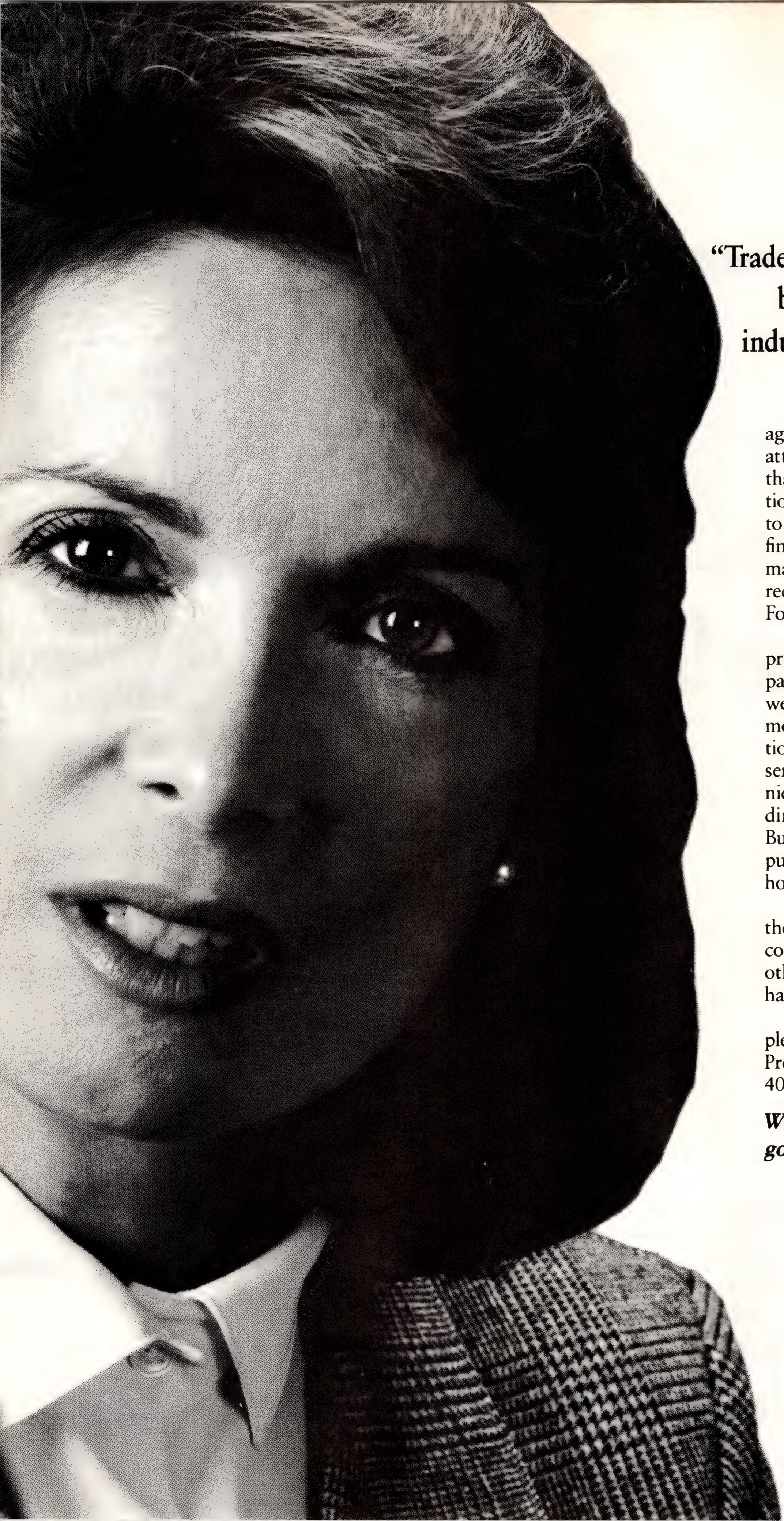

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TECHNOLOGY NEWSLETTER

ALUMINUM-NITRIDE COPPER BONDING IMPROVES MCMS

A proprietary technology that bonds copper layers directly to substrates for use with power ICs has been extended to aluminum nitride (AlN) for multichip-module (MCM) applications. The direct-copper-bonded (DCB) process, developed by IXYS Corp., Santa Clara, Calif., can be applied to AlN to increase the substrate's thermal conductivity. AlN has 500% higher thermal conductivity than does alumina, which dramatically improves the current-handling and power-dissipation capabilities of an MCM. With the packaging technique, power chips can be placed in close proximity with each other, translating into more power density per unit volume. The DCB substrate is the basis for power-chip-on-card technology, and such power modules have fewer vertical layers in their construction for lower thermal resistance and power-cycling capabilities of up to 150,000 cycles. For more information, contact IXYS at (408) 982-0700. *DM*

DSP SYSTEM-ON-A-CHIP TO TACKLE MIMD ARRAYS

Although unveiled late last year, a high-performance digital signal processor developed jointly by Analog Devices Inc., Norwood, Mass., the Massachusetts Institute of Technology, Lincoln, Mass., and Westinghouse Electric Corp., Baltimore, Md., will find a home in multiple-instruction multiple-data (MIMD) array processors. One such experimental array processor, capable of about 7.68 GFLOPS while consuming only about 100 W, will be used by the MIT Lincoln Laboratories in conjunction with Westinghouse. The ADSP21060 array processor will be implemented on an EISA-bus plug-in card holding 64 DSP chips. The processor, fabricated in a 0.6-µm CMOS process, contains 512 kbits of SRAM—the largest memory of any commercially available DSP chip—and delivers 40 MIPS and 120 MFLOPS (peak) at 40 MHz. To get the high memory density, thin-film transistor loads are employed to save cell area. Placing the active loads above the cell keeps the SRAM cell area to 3.6 by 5.85 µm. The chip incorporates a super-Harvard architecture and can hold 16-, 32-, or 48-bit words concurrently in the static memory. On-chip communication ports (six link ports and two serial ports) allow the chip to be used in arrays with minimal external logic. Chips will be set up in clusters of six using a shared local bus, a global memory space, and a unified cluster address space. Multiple clusters can then be combined into a larger array. One additional DSP chip acts a master that sends instructions to all nodes and uses the serial ports to send data to all nodes. Contact Joe Brewer at Westinghouse at (410) 765-1247. *DB*

OPTICAL DRIVES WORK WITH WINDOWS NT

By eliminating software device drivers, optical storage systems developed by Ten X, Austin, Texas, can plug and play with Windows NT as standard peripherals. The optical drives look to Windows NT like standard hard-disk drives. Both NTFS and DOS FAT (file-allocation table) formats are supported with standard OS commands. Without software to install and maintain, no system memory is used. Upgrades and changes in operating system don't affect drive connectivity, and subsystems can be swapped among workstations. Frequently accessed data resides in a nonvolatile data cache, eliminating the need for transfers to or from the optical disk. As a result, data is usually accessed in under 1 ms. Typical compression ratios of 2:1 to 5:1 shrink storage cost per megabyte. Optical subsystems store 650 Mbytes to 38 Gbytes in 5.25- or 12-in. formats. For more information, contact the company at (512) 346-8360. *SVT*

PARTNERSHIP TO YIELD HIGH-LEVEL FPGA TOOLS

A five-year agreement between Synopsys Inc., Mountain View, Calif., and Xilinx Inc., San Jose, Calif., promises to yield a high-level design environment for field-programmable gate arrays (FPGAs). Both companies will focus on reducing the two critical elements of time to market: The time required to complete a design using high-level design-automation tools, and the time it takes to get to production using low-cost user-programmable logic. The resulting design environment will include a bidirectional link between FPGA synthesis and simulation. More specifically, Synopsys will deliver a new release of its FPGA Compiler synthesis software, and Xilinx will ship a new timing-driven FPGA router. FPGA Compiler will forward-annotate synthesis timing constraints to be read by the Xilinx router, which will then partition, place, and route the design to meet those constraints. Also, FPGA Compiler will have a Xilinx file reader so that delays can be back-annotated from their router up to the simulation and synthesis tools. For more information, call Xilinx at (408) 559-7778 or Synopsys at (415) 962-5000. *LM*

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TECHNOLOGY NEWSLETTER

OP-AMP TESTS MEASURE 156 ELECTRONS/MS

How do you economically measure a semiconductor op amp's bias current (I_b) of 10^{-15} A on a production line tester where every second costs money? The only possible way is to integrate it over seconds of time. On top of that, typically ignored error sources—ranging from stray current paths to cosmic rays—can overwhelm low-level measurements. Recently, test engineers at National Semiconductor, Santa Clara, Calif., came up with a solution to this daunting challenge. With a little help from staff scientist Bob Pease, who developed a number of techniques to minimize error sources (ELECTRONIC DESIGN, *Sept. 2, 1993, p. 85)*, they created the LMC6001. Its top grade—the A version—is specified at a maximum bias current of 25 fA. The LMC6001's origins began with National's 660 family of CMOS op amps, announced a few years ago, which had a virtually unmeasurable I_b. These op amps were given a typical I_b of a few femtoamperes, but minimum guaranteed I_bs were specified at a gross 2 pA. However, customers with applications ranging from pH meters to gas detectors soon discovered the 660's real I_b and started screaming for guaranteed bias currents below 0.1 pA. Hence the LMC6001, which is optimized for low-power operation (just 850 µA of quiescent current), yet at the same time minimizes internal heating effects on bias current and offset voltage. To meet this last requirement (called turn-on settling time), a problem with most low-I_b op amps, the top grade's I_b is tested at three intervals during the first five minutes of operation. Any devices that show significant change in offset voltage (350 µV maximum for the A grade) or bias current are rejected even if they meet data-sheet specifications. The LMC6001 isn't a commodity op amp—the A grade in an 8-pin plastic DIP runs $8.50 in 1000-unit lots. The B and C grades specified at I_bs of 100 and 1000 fA maximum, run $5.15 and $1.40 each, respectively, in similar quantities. The A and B grades are also available in hermetically sealed, 8-pin metal cans at slightly higher prices (about $12 for the A grade, $8.50 for the B grade). These devices will compete with J-FET op amps which are only availabale in 8-pin plastic DIPs. Call Mark Cosgrove at (408) 721-6973. *FG*

PROJECT TO YIELD DENSE FLASH CHIPS

Higher-efficiency cell structures that promise flash-memory densities of 16 and 64 Mbits are the cornerstone of a co-development agreement between Hitachi Ltd., Tokyo, Japan, and Mitsubishi Electric Corp., Itami, Japan. Each company developed nonvolatile storage technologies appropriate for high-density flash memories, and will share future R&D efforts as well as production to provide compatible products. From Mitsubishi's research labs comes DINOR, an advanced version of the existing NOR-type cell structure. The cells are smaller than previous NOR cells and can operate and be programmed with low voltages. For example, a DINOR-based memory chip can operate from a single 5- or 3.3-V supply. This cell, which will be used in a 16-Mbit flash memory to be manufactured initially by Mitsubishi, is targeted at working-storage random-access memories. Hitachi will implement a 64-Mbit flash memory with its AND cell. The novel cell uses aspects of both the NAND and NOR structures and permits block erasures as small as 512 bytes. The AND-type architecture is best suited, according to Hitachi, for file-storage and disk-drive replacement applications. The two companies will eventually consolidate their 16- and 64-Mbit product lines so that they offer common specifications and, consequently, get accepted as a de facto industry standard. Additional companies are invited to join the DINOR-AND group. One expected partner is SGS-Thomson Microelectronics, Agrate, Italy, which already has a flash-memory development alliance with Mitsubishi. Contact Mitsubishi's Dwain Aidala at (408) 730-5900, or Hitachi's Ken Mizoguchi at (914) 333-2902. *DB*

FIBER-OPTIC SENSORS TO GAIN MORE ACCEPTANCE

Displacement, position, and proximity sensors, which have previously experienced widespread use across many industrial applications (e.g., packaging and materials handling), are expected to spearhead an overall growth in the acceptance and use of fiber-optic sensors. Flow and chemical fiber-optic sensors also are expected to see greater usage. These observations form the conclusion of a research report compiled by Frost & Sullivan, New York, N.Y., and Mountain View, Calif. The cause for such heightened acceptance comes from a growing demand for low-cost, high-efficiency sensors. Future users of fiber-optic sensors are expected to reap the benefits from their small size, intrinsic safety, and compatibility with other electronic systems and sensors. According to the study, more U.S. and Japanese companies are entering the fiber-optic sensor market, a market which has been dominated by European-based firms. For further information, contact Frost & Sullivan at (415) 961-9000 or (212) 964-7000. *CA*

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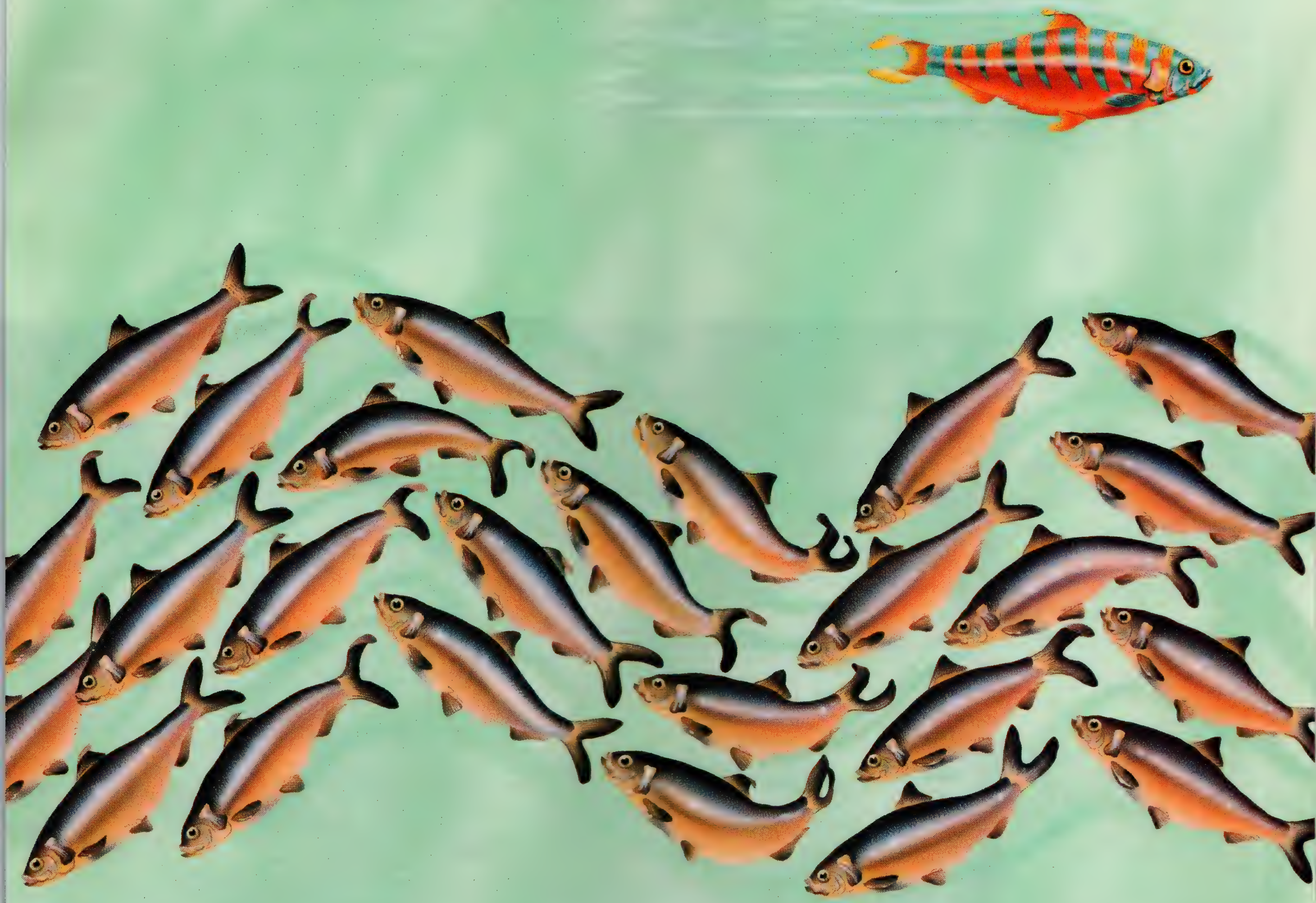

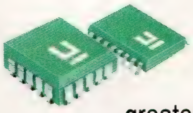

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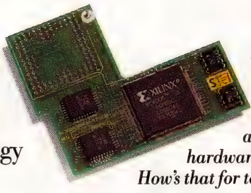

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LCD TECHNIQUE OFFERS ACTIVE-MATRIX PERFORMANCE AT NEAR PASSIVE-MATRIX COST

As notebook-size computers become a commodity item, designers continue to search for ways to improve their computer systems while simultaneously reducing their overall costs. One of the most expensive components of a notebook computer, if not *the* most expensive, is the display, usually a liquid-crystal display (LCD), especially in color systems. Because of their low-power requirements, LCDs have generally been the displays of choice in almost every portable computing application.

Generally, designers of notebook computer systems have had to choose between two kinds of LCDs—active- or passive-matrix types. The former type offers more colorful and sharper images, but it's also more expensive. Now, however, comes a third option—LCDs that use active addressing—a technique developed by Motif Inc., Wilsonville, Ore. (Motif was jointly formed by Motorola Semiconductor Inc., Phoenix, Ariz., and In-Focus Systems Inc., Tualatin, Ore., about 16 months ago). An LCD with active-addressing circuitry produces an image quality approaching that of the active-matrix LCD, but at a cost that's more in line with passive-matrix LCDs.

At the OEM level, passive-matrix LCD color displays typically sell for about $550 apiece while active-matrix models cost about $1200. The use of active addressing techniques, on the other hand, adds about a 35% premium to the price of passive-matrix models, with displays coming in around $750, yet it provides a performance level that's comparable to active-matrix displays. Monochrome active-addressing displays also will be available for around $240 each, which is about 35% more than what passive-matrix-type monochrome displays command in price.

Active addressing of an LCD can keep the costs down because such displays are manufactured by techniques that are similarly used to manufacture passive-matrix-type LCDs. The high yields generally associated with passive-matrix-type panels are passed on to LCD panels that use active addressing .

In an active-matrix-type LCD, the driver and addressing circuitry is placed under each pixel. As a result, the active-matrix-type LCD can be viewed as one huge IC. By moving the electronic circuitry to an ASIC (called active-addressing ICs, or AAICs), as is the case with the active-addressing method, the LCD manufacturing process is simplified which lowers the overall cost.

In an active-addressing display, all of the pixels are driven constantly and simultaneously using external ASICs developed by Motif. In passive-matrix displays, on the other hand, just one row at a time is addressed, causing pixels on other rows to decay or fade *(see the figure)*.

In the new technique, proprietary algorithms are employed to intelligently distribute many small pulses selectively to the desired pixels. The liquid pixels are addressed so rapidly and continuously that they never have a chance to decay between pulses. The result is a color LCD that can display full-motion video without sacrificing contrast or color quality and without introducing any screen flicker.

The only limitation when using the active-addressing technique is that it employs the same base LCD as a conventional passive-matrix-type LCD. As a result, active-addressing technology in general will advance at about the same rate as passive-matrix technology. Passive-matrix-type LCDs continue to improve, though—one 16.7-in.-diagonal display is currently in production.

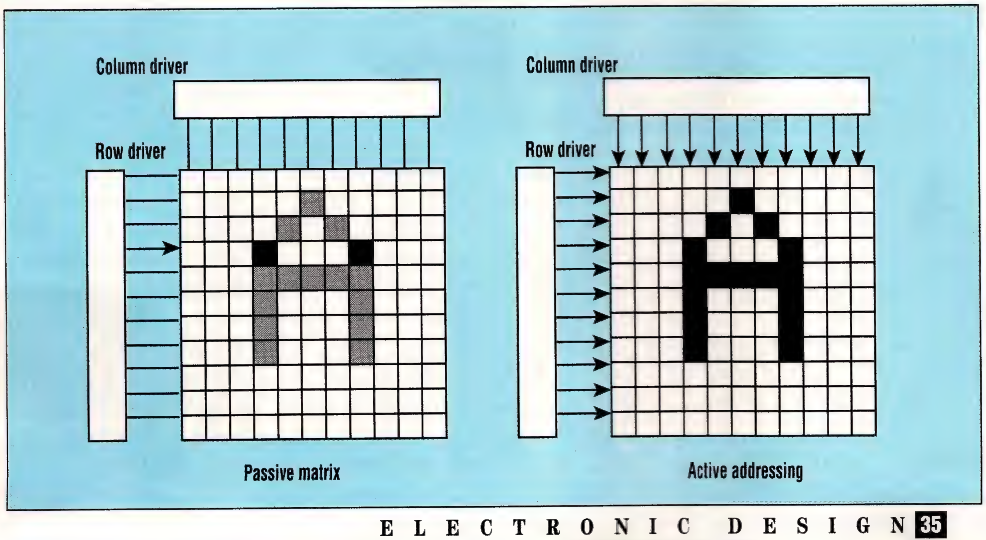
Two implementations of active addressing currently exist: full-line and multiple-line configurations. The full-line configuration scans all rows simultaneously, while the multiple-line configuration scans smaller packets of rows. The full-line method offers higher performance, but it's also more expensive. Multiple-line displays, on the other hand, offer performance that's suitable for lower-cost applications like video games and handheld computers.

Active-addressing LCDs will initially show up in systems that require the high resolution and sharp contrast needed to run multimedia-based software. According to Motif, the active-addressing ASICs should be in production in the second quarter.

The company will sell the ASICs to limited partners, and will also offer complete displays on the open market. The displays will be available for shipping soon after the chips are manufactured and are ready.

For more information on the active-addressing technique, contact Motif at (503) 682-7700.

RICHARD NASS



THE ITU EXAMINES THE RELIABILITY OF CCSS #7 AMID REPORTS OF ISDN CRASHES

During the past year and a half, the Integrated Services Digital Network has experienced a series of dramatic crashes. Now the Telecommunications Standardisation Bureau (TSB), part of the International Telecommunications Union (ITU), Geneva, Switzerland, has stepped in to try and rectify the problem. The TSB has invited all telecommunications network operators, equipment manufacturers, and scientific and industrial organizations to contribute in an investigation into the reliability of the Common Channel Signaling System No. 7 (CCSS#7).

CCSS#7 is crucial to the operation of ISDNs, passing signaling and control information between central-office switches and to customer terminal equipment. Most important is the interconnection between ISDNs run by different telephone companies and over long-line carriers. The signaling system was defined by the ITU and has been adopted by all network operators throughout the world.

Wendal Harris of the U.S. Federal Communications Commission (FCC), Washington, DC, confirmed that since October 1992, there have been 27 serious "outages" of CCSS#7-based networks, all but six of them in the United States. Harris defines an outage as a "discontinuity of service that affects more than 50,000 users for a period longer than one hour." Harris is chairman of the TSB's Study Group 11, formed at his suggestion specifically to monitor technical problems with CCSS#7.

So far, according to Harris, the findings seem to indicate that all but four of the reported crashes were a result of either hardware failure, a software bug, or human error. "That implies that the problems were caused by implementation errors," he says. As a result, Harris sees no need for the specification to be amended significantly.

Industry insiders have a less diplomatic view. They suggest that the blame lies with hardware suppliers. In addition, they allege that some vendors test software only with simulated traffic before commissioning their systems. Thus, their systems could become overloaded without warning and crash at peak times. With little or no margin for error, network controllers need to be very highly skilled or be given very advanced network management tools to predict and avert overload situations.

Harris says that outage reports submitted to his study group have to include details of what actions were taken to cure the problem. "In many cases, the solution for a particular operator was to enhance training standards for operations personnel," he says.

Another industry view is that different interpretations of the CCSS#7 recommendation by manufacturers have led to incompatibilities between their products. These observers say that failures have occurred at "signaling transfer points."

Harris admits that differences of interpretation and implementation do exist. But he stresses that CCSS#7 is a very complex and sophisticated technology which introduces a number of new features to public switched networks, such as in-band signaling. He also points out that some manufacturers have had to adapt older products to use the system.

Harris adds that it's not ITU policy to identify either the network operators or equipment suppliers involved in a network failure. However, he's prepared to agree that reports gathered so far indicate a fault in networks is more likely if there are a variety of systems provided by different manufacturers. This is also highlighted by the relatively low number of outage reports from outside the United States, where network operators tend to use fewer systems from a smaller number of equipment vendors.

Manufacturers and network operators confide that catastrophic failures meeting Harris' "significant outage" definition don't reveal the whole picture. Borrowing jargon from the electrical power industry, they claim that more "brownouts" have occurred, where despite a signaling-system failure, a network was kept operational but at much reduced efficiency.

Now the ITU wants to widen the range of expertise available to examine the problem. Harris explains that until recently, outage reports were circulated only to recognized operating agencies or telephone companies, as well as national administrations. However, Study Group 11 also includes manufacturers. The group believes they could contribute better to finding a solution if they also received the reports. As a result, all scientific and industrial organizations with an interest in the topic are invited to participate in the investigation.

PETER FLETCHER

MCM-D TECHNOLOGY FUELS NOTEBOOK WORKSTATION

Although advanced RISC-based workstations have long been touted as a fertile breeding ground for a large-volume multichip-module (MCM) implementation, the actual use of MCMs in RISC workstations has struggled to get off the ground. That's basically due to the same reasons which caused delays in the development of the overall MCM market: known-good-die issues, test dilemmas, and perceived cost and difficulty barriers.

The ice finally was broken, though, by one of the first companies to commit to an MCM implementation of a RISC chip set. Ross Technology Inc., Austin, Texas, in conjunction with nChip Inc., San Jose, Calif., created an MCM implementation of the Ross Sparc chip set that's now in volume production in the Sparcbook 2, the notebook-sized equivalent of a Sparcstation 2. Moreover, a second-generation version of the MCM is on the way.

The Sparcbook 2, which is being built by Tadpole Technology Inc., Austin, contains an MCM that incorporates a Sparc integer

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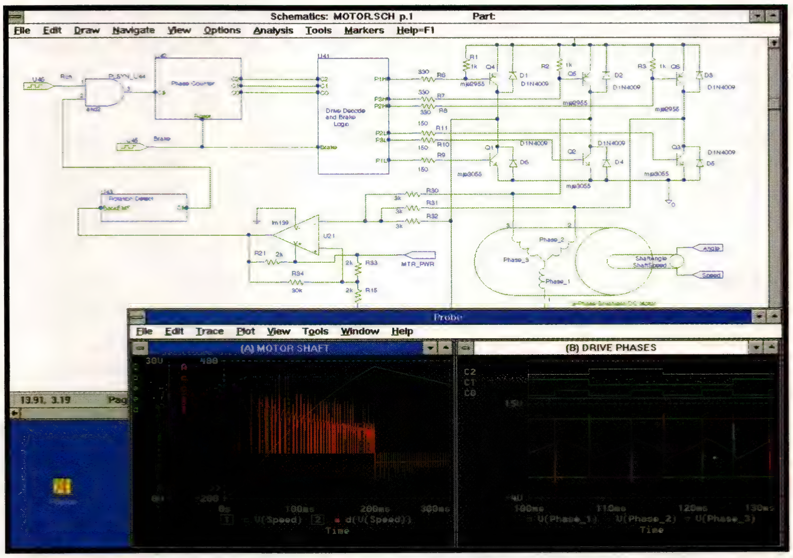
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• Circle No. 305 for IBM • Circle No. 306 for SPARCstation • Circle No. 307 for Macintosh unit, a floating-point processor, a cache controller and memory management unit, and two cache RAMs. Aside from a substantial size reduction, integrating these devices on an MCM allows very high yields to the chips' top speed grade (40 MHz), reduced power consumption, and a lower unit-production cost than the pc-board-packaged version the MCM replaces.

The module, designated model CYM6111, is packaged in a 45-mm^2 ceramic quad flat pack (QFP) with 256 leads on a 0.65-mm pitch. The MCM's substrate, which is fabricated in nChip's nC1000 silicon-dioxide technology, measures 25.4 by 31.5 mm. Because many interconnections are made within the substrate itself, the MCM requires less than 100 external I/Os, even though the ICs contain over 400 signal pads. The remainder of the QFP's leads are used for power and ground or test points, or they act as dummies.

Originally, the Ross Sparc chip set was packaged as individual chips and marketed on pc boards as a card-level CPU for Sun Microsystems and other customers. However, the chip set was partitioned with MCM implementation in mind. The MCM version's total packaging cost is equal to or lower than the discrete-chip version. It includes 64 kbytes of zero-wait-state RAM and offers performance of 32 sustained MIPS or 28 SPECmarks at 40 MHz.

Because the substrate technology uses silicon dioxide as a dielectric, no thermal vias are required and signals are routed freely under the dice. The module's thermal resistance of 0.9°C/W permits operation in the fan-less environment of the notebook computer. The module has 1264 wire bonds with a minimum wire-bond pitch of 150 mm.

The expected benefits of MCM implementation are realized in this conversion. Several nanoseconds of processor cycle time were cut thanks to shortened interconnects and lighter capacitive loads. Clock skew and worst-case address-bus delay were cut to 230 ps and 400 ps, respectively.

Power consumption is reduced as well. The module dissipates 5 W and, although no controlled experiments have been done, Tadpole estimates power savings at 20 to 30%. The module offers improved power distribution to the ICs. It incorporates full power and ground planes plus an integral decoupling capacitor. The maximum dc drop between chips in the module is 1.5 mV and maximum ground bounce was measured at 65 mV. With its power-distribution structure, modules are functional at full speed even with only four power/ground wire-bond pairs (one per substrate side) in place.

MCM packaging also offers benefits at the next level of assembly. There are 333 signals from the ICs in the module that never leave the substrate, and only 75 (the Sun Mbus signals) that

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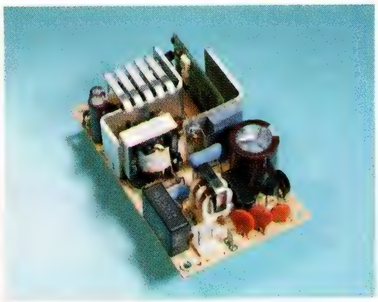
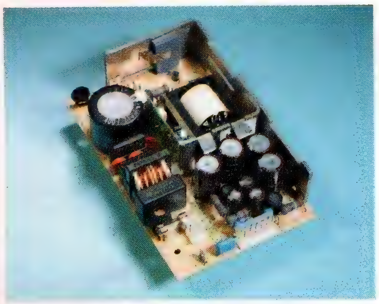


3"x5" Footprint 40W
Model KRW 352KV



3.94"x6.3" Footprint 65W
Model MRW 171KV

MODEL	POWER	OUTPUT #1		OUTPUT #2		OUPTPUT #3	
	Watts	Volts	Amps	Volts	Amps	Volts	Amps
KRW 350KV	40	+5	0.5-3.0 (typ) (4.0 max)	+12	0.3-2.0 (typ) (3.0 max)	-12	0-0.1 (typ) (0.3 max)
KRW 351KV	40	+5	0.5-3.0 (typ) (4.0 max)	+15	0.3-1.6 (typ) (2.0 max)	-15	0-0.1 (typ) (0.3 max)
KRW 352KV	40	+3.3	0.5-3.0 (typ) (4.0 max)	+12	0.3-2.0 (typ) (3.0 max)	-12	0-0.1 (typ) (0.3 max)
MRW 150KV	35	+5	1.0-2.2 (typ) (4.0 max)	+12	0.6-1.8 (typ) (2.5 max)	-12	0-0.1 (typ) (0.3 max)
MRW 151KV	35	+5	1.0-2.2 (typ) (4.0 max)	+15	0.6-1.4 (typ) (2.0 max)	-15	0-0.1 (typ) (0.3 max)
MRW 160KV	50	+5	1.0-5.0 (typ) (6.0 max)	+12	0.5-2.0 (typ) (2.5 max)	-12	0-0.1 (typ) (0.5 max)
MRW 161KV	50	+5	1.0-5.0 (typ) (6.0 max)	+15	0.5-1.5 (typ) (2.0 max)	-15	0-0.1 (typ) (0.4 max)
MRW 170KV	65	+5	0.8-5.0 (typ) (7.0 max)	+12	0.3-1.7 (typ) (2.5 max)	-12	0.3-1.7 (typ) (2.5 max)
MRW 171KV	65	+5	0.8-5.0 (typ) (7.0 max)	+15	0.3-1.3 (typ) (2.0 max)	-15	0.3-1.3 (typ) (2.0 max)

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require connection outside the module. Thus, the MCM reduces the number of connections that must be routed on the pc board by 80%.

Ross and nChip have gone on to develop a second-generation Sparc MCM. Based on Ross' Hypersparc architecture, the new module will run at 72 MHz and offer twice the performance of the original 40-MHz version in most applications. The upgraded version is footprint-compatible with the CYM6111 module.

According to Ross' president and c.e.o., Roger Ross, the company's earlier experience with MCM implementation made the new development process run smoothly. "The Hypersparc design went from net list to tested prototypes in seven weeks with first-pass success at each step," says Ross. Based on the two successful MCM developments, Ross and nChip are planning two more generations of Sparc MCMs. Those modules will be fabricated by Fujitsu in 0.5-mm CMOS technology and will feature processor clock rates extending to 100 MHz and more.

For more information about the Ross Sparc MCM-D implementation, contact Ross Technology's Steve Goldstein at (512) 892-7802, ext. 519.

DAVID MALINIAK

PACKET-SWITCHING BUS PASSES 64-BIT DATA AT 320 MBYTES/S

Typically, high-end computer-board and system data-transfer options top out at a word width of 32 bits. Examples include the VMEbus, the EISA bus, and other standard buses. Some 64-bit-wide buses have emerged, such as the VME64 bus, which has a maximum data-transfer rate that's limited to 80 Mbytes/s.

Now the data-transfer rate has been raised thanks to the development of the SkyChannel bus from Sky Computers Inc., of Chelmsford, Mass. The SkyChannel can pass 64-bit-wide data, either within a computer board or from a computer board to a computer board, at a rate of 320 Mbytes/s. Using the maximum 256 9U-size computer boards (with a total of 4096 microprocessors), a throughput performance level of 320 GFLOPS can be achieved.

The SkyChannel bus achieves its high speed by passing data that's packet-switched, rather than circuit-switched, or passing token-ring data that's employed on competitive buses.

In a packet-switched write operation, the transmitted packet contains both the destination-address information (routing information) and the data. The bus is then released to send

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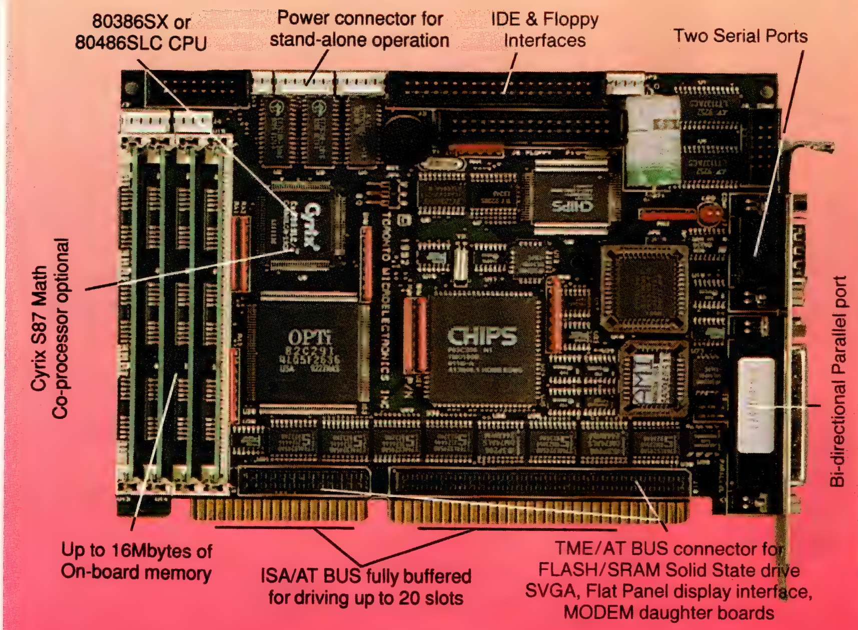
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TME's F486SLC		COMPETITOR
✓	80386SX	Yes
✓	80486SLC	?
✓	16/25/33/40Mhz	?
✓	Up to 16 Mbytes of On-board memory	Yes
✓	64K Write back cache	No
✓	Two serial ports with 10KV ESD Protection	No
✓	One Parallel Port	Yes
✓	Floppy & IDE interface	?
✓	Under 6.5W capability	?
✓	Watch Dog Timer	?
✓	Power Fail Detection	No
✓	Small form factor 4.75" x 7"	?
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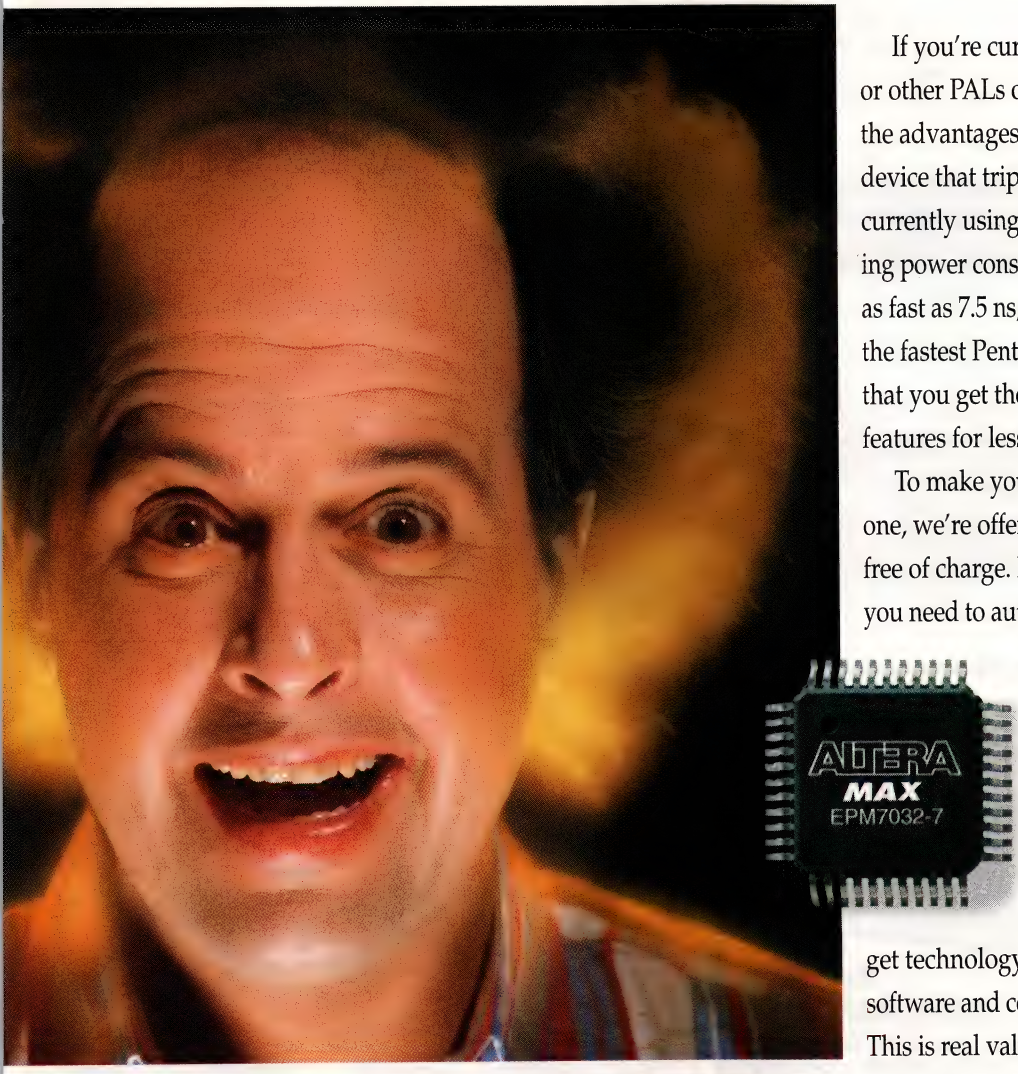

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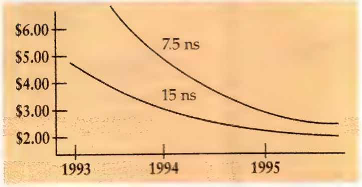
Tpd = 10.0 ns	$ 7.95	$ 9.90
Tpd = 7.5 ns	$11.95	$14.25

Above prices are based on 100 piece quantities. Pricing for the 22V10 is based on the lowest of the published prices from Lattice and AMD as of January 1, 1994.



EPM7032 projected 25,000 unit pricing through 1995.

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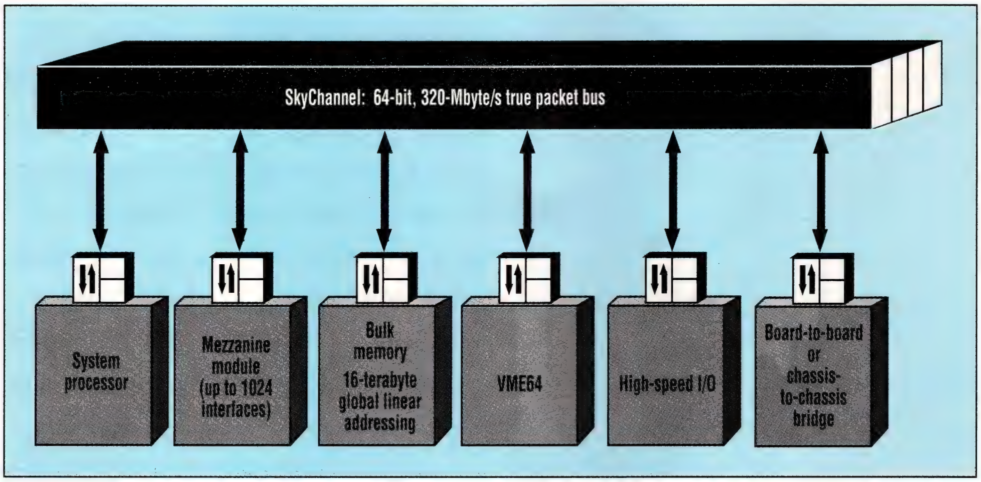
more data.

As it establishes a path between processors by sending data packets between FIFO buffers at each interface, this method eliminates any delays encountered. The read operation works in a similar fashion. No processor cycles are required for the handshaking operation. Data and address words supply 44-bit-wide global addressing. Programming is simplified using a 16-terabyte global-addressing space. In addition, a broadcast capability is available to every attached interface.

In a circuit-switched bus, the bus is held during periods of inactivity, causing a delay. While in a token-ring scheme, read and write latencies exist as a path is being established.

Most traditional architectures are limited by the speed of the slowest I/O device. However, over the SkyChannel bus, all packet-switched data bursts are sent at the maximum bus speed. Data transfers are accelerated by buffering the CPUs and global memory from the slower I/O devices. The bus is held only during data bursts. In addition, bus efficiency increases as more processors are added.


SkyChannel: 64-bit, 320-Mbyte/s true packet bus
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VME64
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The SkyChannel bus can be connected directly to the system CPU. Moreover, it's able to interface with a mezzanine bus, the system memory, the VME or VME64 bus, or other high-speed I/O ports *(see the figure)*.

All SkyChannel bus interfaces are implemented uniformly and independently. This modular architecture offers a migra-

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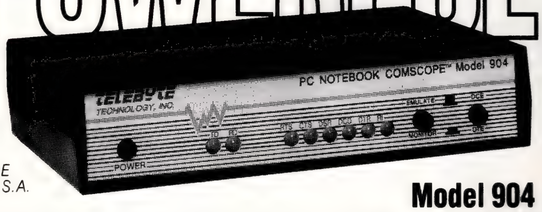

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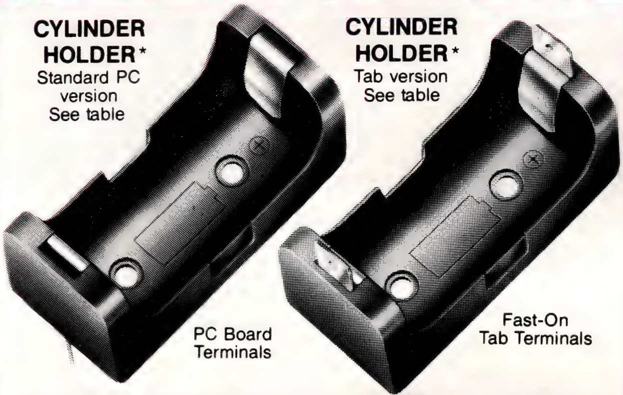

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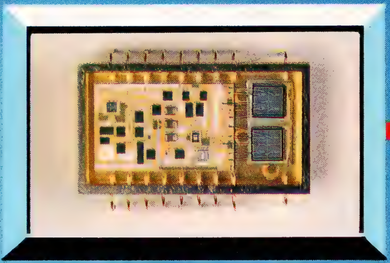
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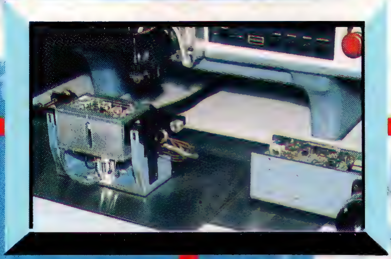
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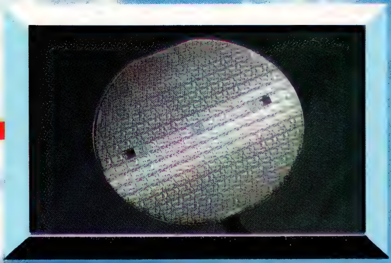
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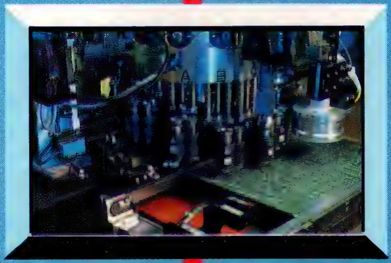
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tion path to future upgrades and allows for a heterogeneous environment.

The SkyChannel bus is an open specification that's been proposed to the VFEA International Trade Association (VITA) as a communications standard for VMEbus-based systems.

Also available from Sky Computers is the SkyChannel Design Guide. This guide includes the complete protocol specifications, a design example with hardware schematics, software code, and Verilog simulator models.

The modular SkyBolt II family is one example of boards that can take advantage of the SkyChannel bus architecture. The family employs the SkyBolt II motherboards and Shamrock II daughtercards. Each daughtercard contains four RISC microprocessors, and either 16 or 64 Mbytes of RAM. The 6U baseboard, which holds one Shamrock II board, delivers a performance of 320 MFLOPS. Four Shamrock II cards are in the 9U version, which pumps out data at a performance level of 1.28 GFLOPS.

Each SkyBolt II motherboard is built with an i960CA microprocessor. The microprocessor manages the I/O list processing and scheduling, freeing the daughtercard for computation.

SkyChannel desktop accelerators are also available. One such accelerator is the SkyStation II. This plug-and-play, SCSI-based workstation accelerator can deliver 640 MFLOPS of throughput using a pair of Shamrock II daughtercards and 512 Mbytes of system memory.

The high speed of the SkyStation II accelerator makes any system that's based on it suitable for medical imaging applications.

Users also can obtain fully-configured and ready-to-run systems, called the SkySystem. The SkySystem, built with SkyBolt II boards, comes with the Solaris operating system, a monitor, a hard-disk drive, a CD-ROM drive, and various software utilities.

For more information on the SkyChannel, SkyStation II, or SkyBolt II, call Sky Computers at (508) 250-1920.

RICHARD NASS

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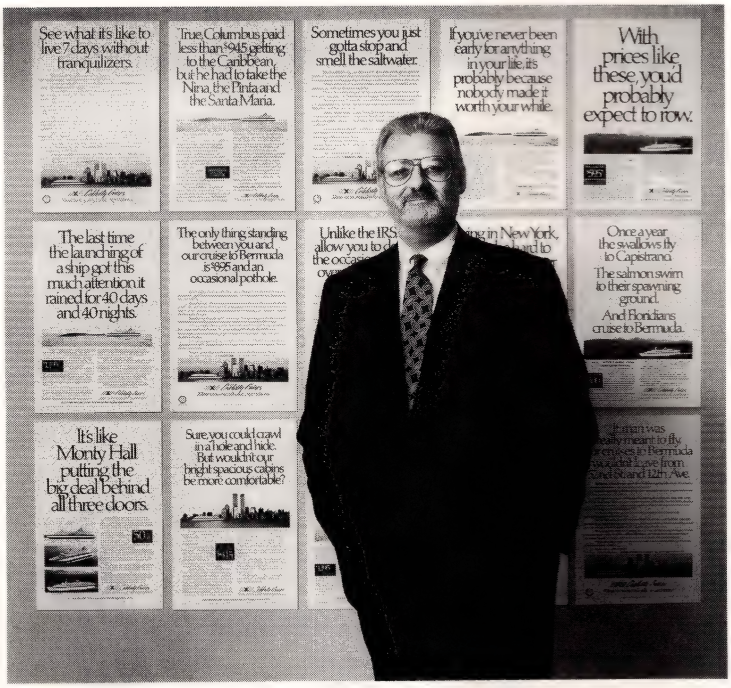
What are we going to do with your extra robots, Fenton?
Maybe a small college football team needs a new front line!

"Increasing our ad budget was so successful, our agency recommended we cut it."

Photo: Frank Moscati


See what it's like to live 7 days without tranquilizers.
True, Columbus paid less than $945 getting to the Caribbean, but he had to take the Nina, the Pinta and the Santa Maria.
Sometimes you just gotta stop and smell the saltwater.
If you've never been early for anything in your life, it's probably because nobody made it worth your while.
With prices like these, you'd probably expect to row.
The last time the launching of a ship got this much attention it rained for 40 days and 40 nights.
The only thing standing between you and our cruise to Bermuda is $695 and an occasional pothole.
Once a year the swallows fly to Capistrano. The salmon swim to their spawning ground. And Floridians cruise to Bermuda.
It's like Monty Hall putting the big deal behind all three doors.
Sure you could crawl in a hole and hide. But wouldn't our bright spacious cabins be more comfortable?

Al Wallack, Sr. VP Marketing, Celebrity Cruises, after returning from having his hearing checked.

"A great time to introduce a new luxury cruise line. The economy was in a slump, and the competition was on the rise.

We told our new advertising agency we have to go in with all guns blazing. And gave them the extra money to do it.

They recommended a three phase campaign. Phase 1. Full page newspaper. One ad a week for 24 weeks and one-third pages in the travel section. Phase 2, radio. Then 3, television to sweep up one season and sow the seeds for the next.

To make a long story short, two-thirds into the newspaper phase, Celebrity's ships were just about full to the end of the season. With so little left to sell, we all agreed to hold the radio and TV and save the remainder of the budget.

In roughly two years Celebrity became the number one cruise line from New York to Bermuda.

We've just added another new luxury ship and we're anxious to fill it. So once again we've upped our budget. So far, our agency hasn't tried to talk us out of it."

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We get that sort of comment all the time. People are impressed that our free Consumer Information Catalog lists so many free and low-cost government booklets. There are more than 200 in all, containing a wealth of valuable information.

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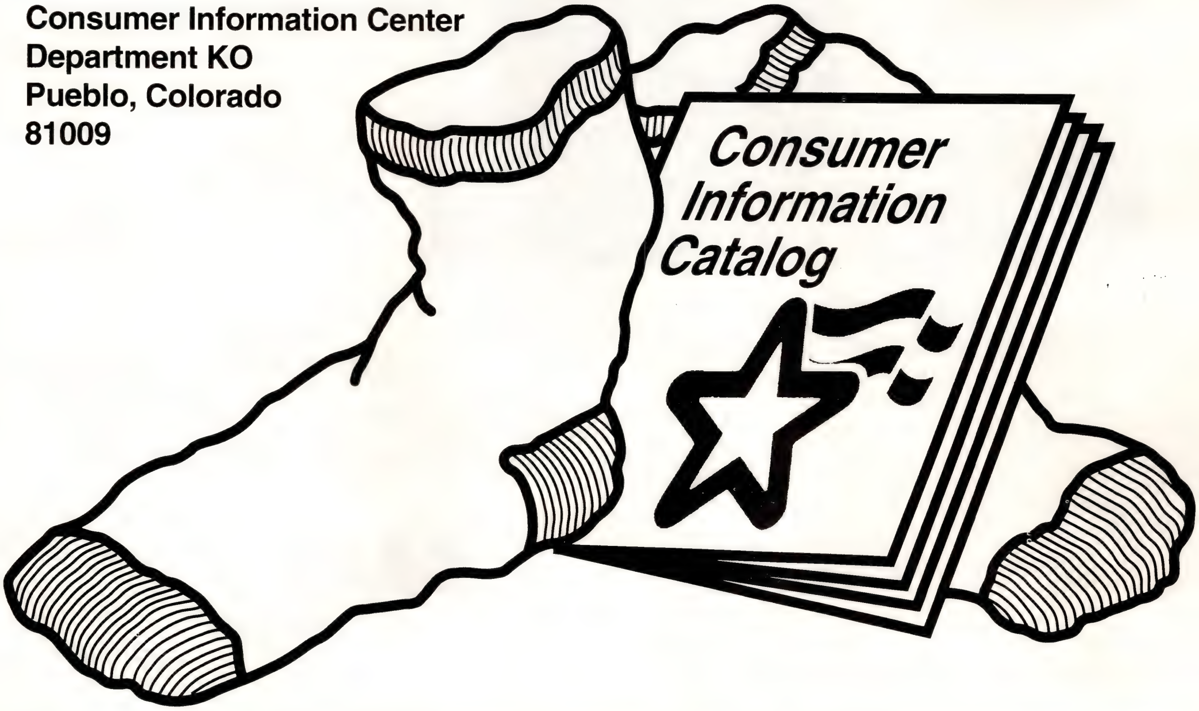

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"Without advertising, everybody would think Ronald was just the name of a former president."

Mike Quinlan, Chairman, CEO McDonald's (left)

"The remarkable thing is, when you think about McDonald's® you've got to think about people. A friendly crew person welcoming you. Kids, moms and dads having a good time at McDonald's, even a funny clown named Ronald.® Those pictures in your mind are advertising at work.

Our advertising is people to people—an invitation from our people to our customers to come in and visit. Personal, friendly, and above all, real.

I'm told there are business people out there who don't believe in the power of advertising. For them, two facts: First, McDonald's is one of the most advertised brands on this planet. Second, McDonald's is the only company listed in the current Standard and Poor's 500 to report combined increases in revenues, income, and earnings per share for more than 100 consecutive quarters since 1965.

Frankly, Ronald and I like to think there's a connection here."

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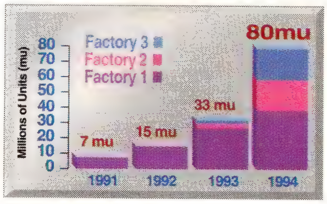
We not only have a ton of these

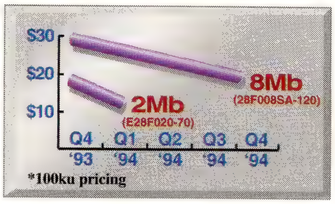
Intel Flash Memory is shipping in high gear. Our factory capacity is up. Our prices are coming down. And we're leading the industry in flash technology.

The shortage is over. With three flash factories now on line, Intel can support both your immediate and long-term needs. In fact, our sub-micron process in each factory allows us to provide multiple sources for our flash products to ensure delivery.

Intel Flash Memory Factory Output



Intel Flash Component Pricing Trend*



*100ku pricing

What's more, our new capacity is so huge, we'll outsupply all other flash manufacturers. Combined.[†]

We're also growing the market by driving down flash prices, making Intel Flash

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© 1994 Intel Corporation. [†]Based on 9/93 Dataquest forecast of total flash units to ship in 1994.

but now you'll also save a ton.

Memory a viable option for virtually any new design. In fact, since Q4 '93, we've dropped prices by as much as 31 percent. And by the end of the year, the volume price for our 120ns, 8Mb FlashFile™ devices will be as low as $20.

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So if you're ready to load up on flash memory, call 1-800-879-4683, ext. 101 for complete information. Because Intel is more than ready to deliver.

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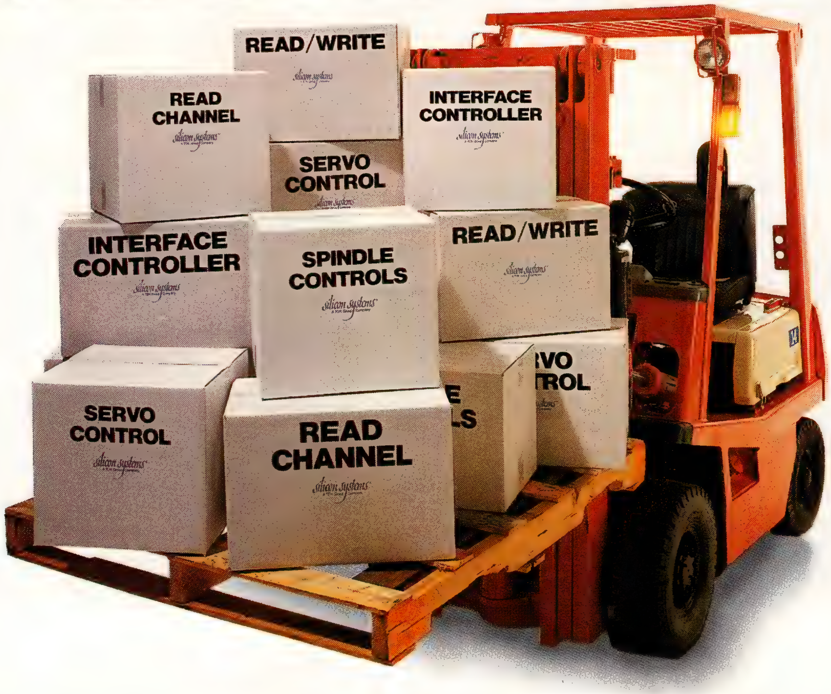

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CONDENSE SYSTEM LOGIC WITH HIGH-DENSITY CPLDs

DAVE BURSKY

The demand for competitive performance among programmable logic users has seen higher-capacity devices swallow the smaller logic circuits that are scattered across a circuit board. In fact, complex programmable logic devices (CPLDs) are already starting a feeding frenzy on 20- to 28-pin PLDs to reduce board clutter and improve system performance. However, many current-generation CPLDs and field-programmable gate arrays (FPGAs) don't have the features needed to easily replace groups of smaller PLDs, such as very predictable timing, short propagation delays, and high utilization. These limitations were met by Cypress Semiconductor in its new high-density CPLD family—the Flash370 series. The new family features short (10 ns maximum) propagation delays for worst-case paths, allowing chips to deliver system speeds of 100 MHz.

In addition, the higher-end family members will have close to double the gate-equivalent capacities of virtually any currently available CPLD, as estimated by the PREP benchmark suites. All members also possess a simple architecture that has no "hidden" delay constraints, providing an easy-to-compute timing model.

The Flash370 series will include seven initial members—the Flash371 through Flash377 (the CY7C371 to CY7C377). They range in pin count from 44 to 288 pins (32 to 256 I/O pins). The chips also contain from 32 to 256 macrocells, 44 to 268 flip-flops, and 6 dedicated inputs (two inputs can also serve as clock inputs on the C371 to 373, and four on the C374 through 377). All chips are electrically erasable and reprogrammable with a 12.5-V programming level, making them reusable

during prototyping or reconfigured in the system. That ultimately reduces both system development and maintenance/upgrade costs. The chips are fabricated in Cypress' 0.65-μm electrically reprogrammable flash CMOS process.

The design tools, combined with the high routability of the interconnection matrix on each chip, permits designers to set up any desired set of pin assignments without sacrificing utilization or increasing the input-to-output propagation delay. Furthermore, even if the internal logic configuration must be modified, the on-chip routability allows pin assignments to be maintained. One propagation-delay specification on the Flash370 applies for any path of up to 16 product terms on one output. Designers don't have to know circuit fan-outs, which inputs are used, or what resources are used. Just like the popular 22V10 PLD, delay properties can be read right off the data sheet.

To make the chips still more flexible, an intelligent product-term allocator that can allocate anywhere from 0 to 16 product terms to any macrocell was added. As a result, the product terms can be steered on an individual basis, and designers can then modify one path without disrupting another to redistribute the terms. In other CPLD families, the product terms are typically steered in groups of four or five. Therefore, if one macrocell needed just one more product term, all of the product terms from a neighboring macrocell must be steered over, often stranding that other macrocell and rendering it useless.

Furthermore, product terms can be shared among nearby macrocells, taking advantage of multiple outputs with common product terms. The sharing feature of the Flash370 series alone provides between 15 and 25% more capacity than implementations without sharing.

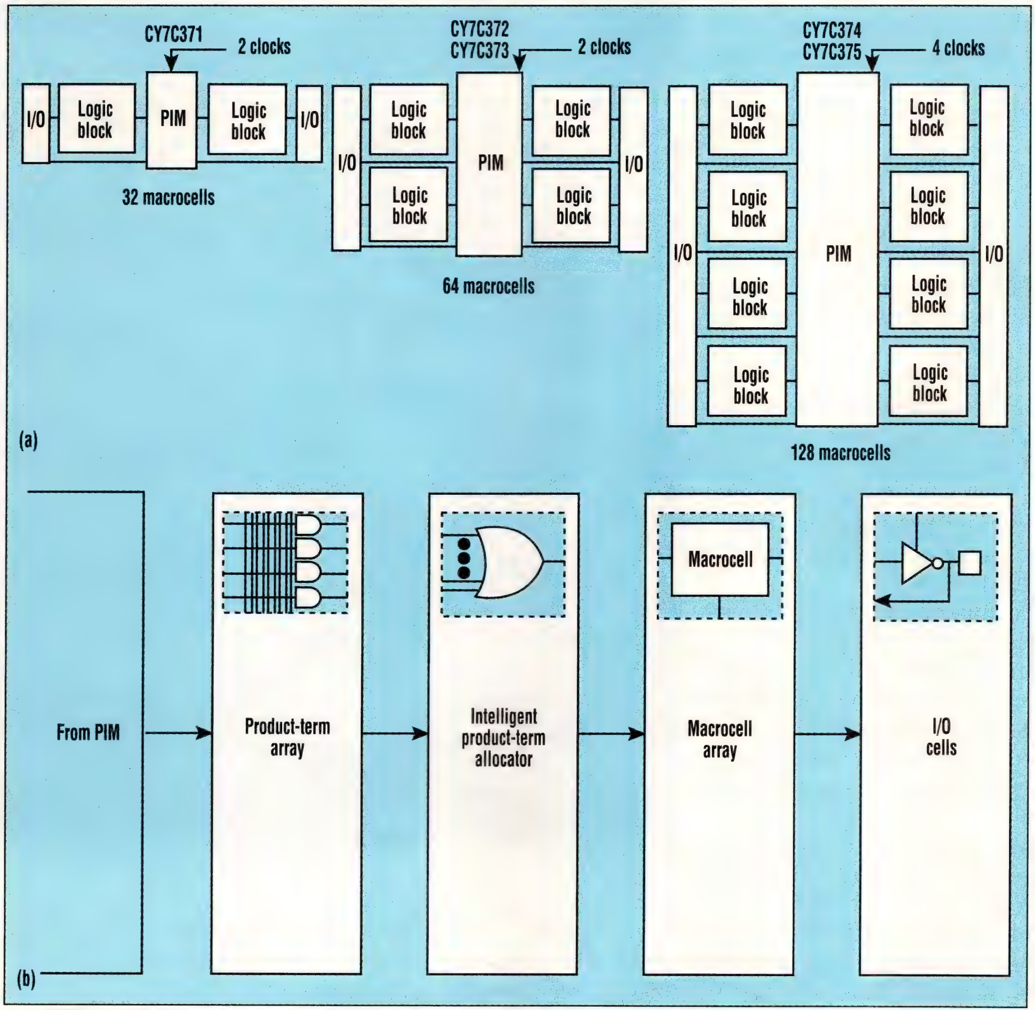
The Flash370 family architecture is very straightforward—each chip in the family contains configurable logic blocks that surround a programmable interconnect matrix *(Fig. 1a)*. Each logic block incorporates its own product-term array, product-term allocator array, 16 configurable macrocells, and the I/O cells *(Fig. 1b)*. The programmable interconnect matrix (PIM) ties the blocks together and also interconnects the blocks to the I/O pins.

The PIM ultimately provides a uniform, predictable delay from block to block, independent of the routing. There's no delay penalty when routing signals through the PIM. Moreover, there are no internal fan-out delays, expander delays, dedicated versus I/O pin delays, penalties for using all 16 product-term inputs on a macrocell, or delay penalties for steering or sharing product terms. Each signal has at least six to seven chances to route for each logic block—more than double the number of path options versus other CPLD families.

Input and output signals as well as the block-to-block signals are all routed and distributed through the PIM. Multiple clock pins (two on the Flash 371, 372 and 373, and four on the 374, 375, 376, and 377) are also available on the chips. This allows different sections of the chip to operate at different speeds. Multiple clock inputs also let designers more evenly distribute the clock signals and balance signal loading.

PACKAGING OPTIONS

To give designers a choice of density and I/O options, each density (except for the smallest chip, the Flash371) will offer two packaging options—one that's I/O intensive and another that's register intensive. In the register-intensive versions, half of the macrocells are "buried" and don't have an I/O



1. THE SIMPLE ARCHITECTURE of the Flash370 family CPLDs developed by Cypress Semiconductor—the logic blocks surrounding the programmable interconnect matrix (PIM)—belies the highly efficient features and high density offered by the various family members (a). Each logic block contains 16 macrocells as well as a very flexible product-term allocator. The allocator incorporates sharing and steering logic that allows from 1 to 16 product terms to be assigned to any output (b).

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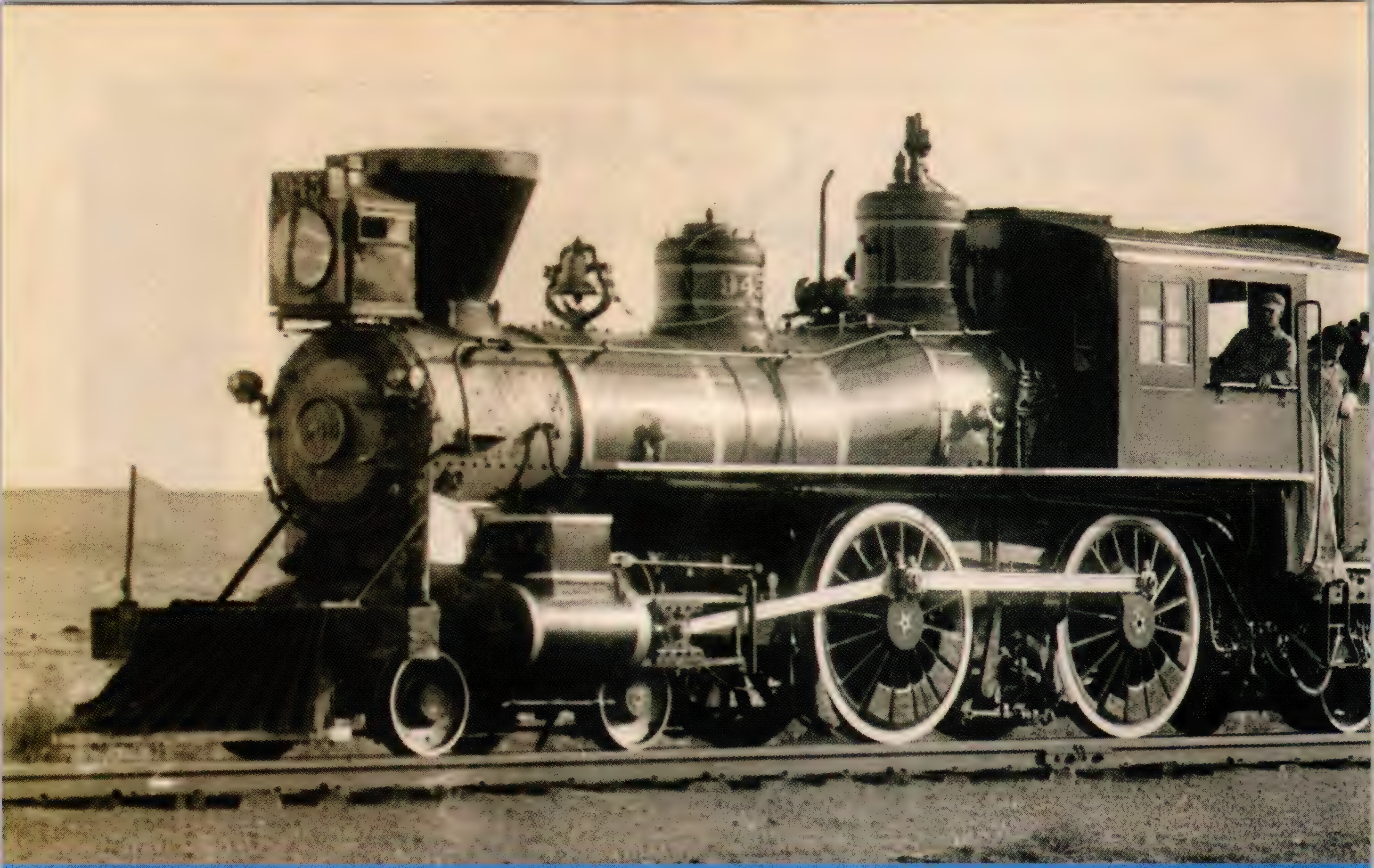

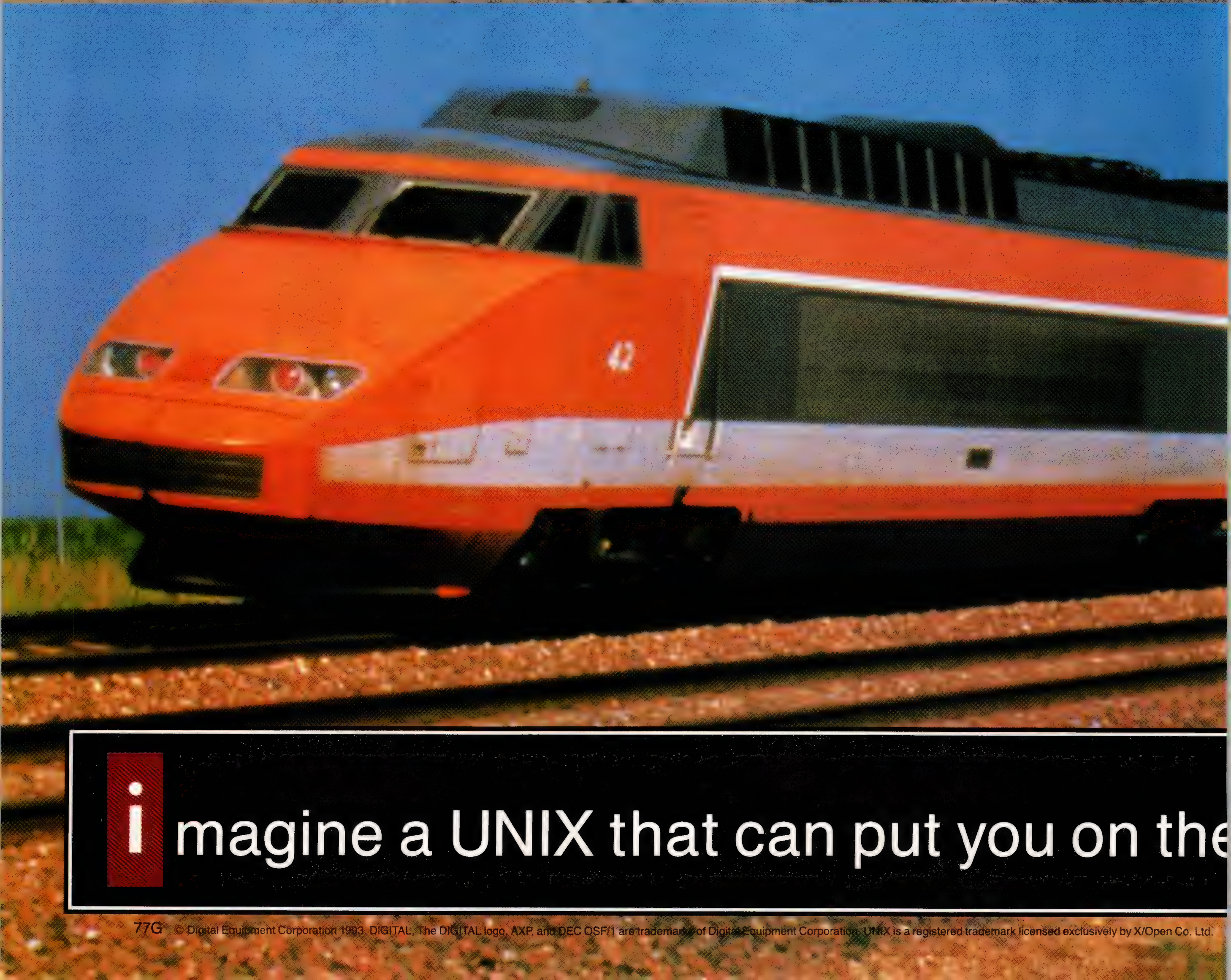

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PUTTING IMAGINATION TO WORK

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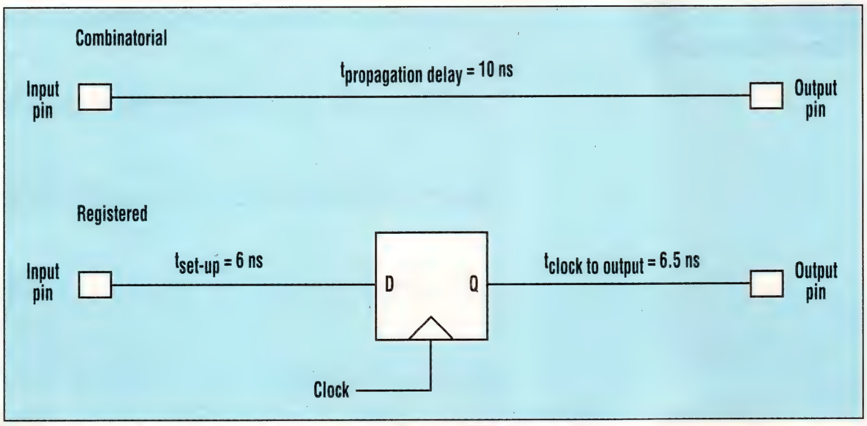

Combinatorial
Input pin
$t_{\text{propagation delay}}$ = 10 ns
Output pin
Registered
Input pin
$t_{\text{set-up}}$ = 6 ns
D
Q
$t_{\text{clock to output}}$ = 6.5 ns
Output pin
Clock

2. BECAUSE THE DELAY THROUGH THE PIM is negligible, the timing model for the Flash370 CPLDs is very simple. For combinatorial functions, it's just a 10-ns delay from input to output for a single level of logic. Registered or clocked functions require a 6-ns setup time and have a 6.5-ns clock-to-output delay, but can run at a maximum clock speed of 110 MHz.

pin associated with them. The buried cells are typically used for state machines and registered feedback paths that aren't required to send a signal to the outside world.

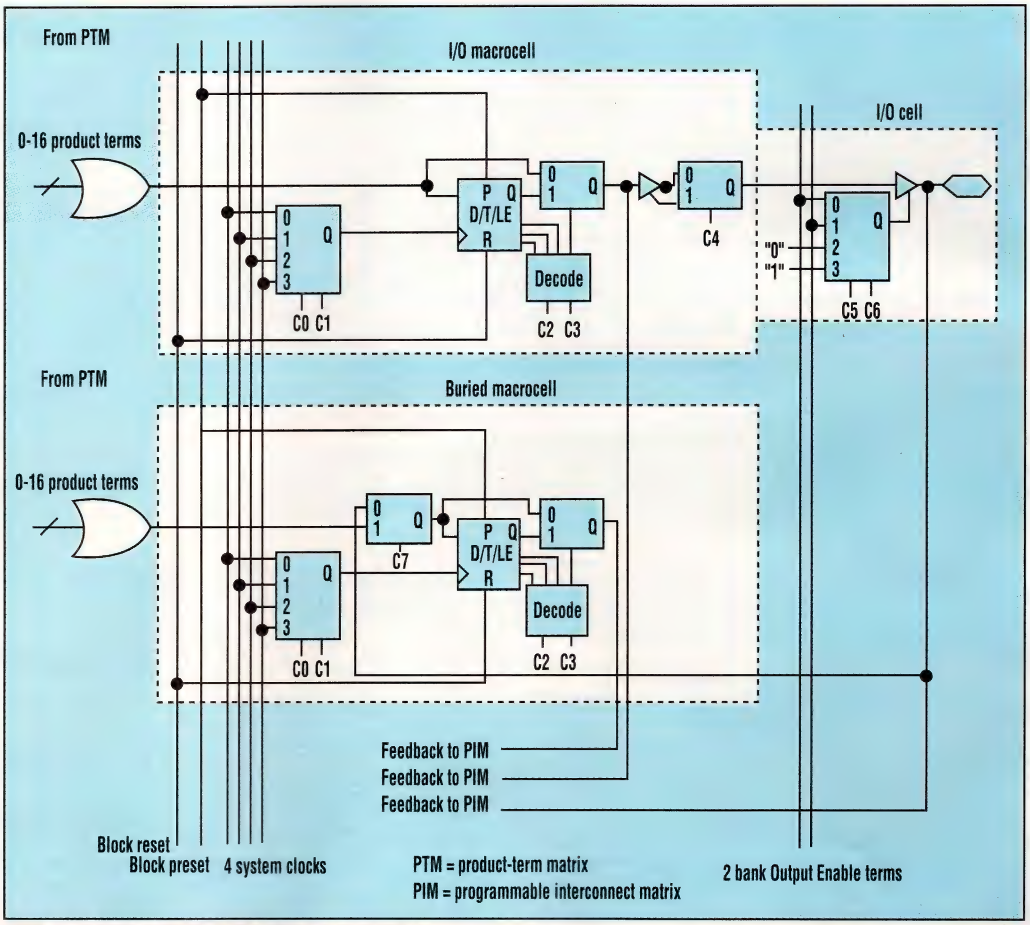
Inside the PIM is a fully global routing matrix for signals from I/O pins and feedback paths from logic blocks. Because the PIM's architecture was developed to be highly robust, it avoids the fitting and density limitations that have constrained other CPLD and FPGA choices. Thus, the chip will permit 100% fully automatic placement and routing without any routing-dependent timing parameters.

Also, the simple architecture of the Flash370 series combined with the predictable timing lets designers use a very simple timing model. The model has a worst-case pin-to-pin propagation delay of just 10 ns for one combinatorial-logic level. For register-based logic, designers can operate at 110-MHz speeds, guaranteed *(Fig. 2)*.

For immediate development needs, the currently available Warp 2 design suite can be used. That suite provides fully automatic logic synthesis and fitting from IEEE 1076 behavioral VHDL design descriptions as well as simulation and timing-analysis tools. A new suite of development tools coming out next month will add schematic-capture support, enhanced timing-simulation support, and support for the pASIC family of FPGAs.

Inputs to the PIM include all I/O and dedicated input pins, and all macrocell feedback lines from within the configurable logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. Signals from any pin or logic block can be routed to any or all logic blocks. The outputs from the PIM are signals routed to the appropriate logic block(s). Each block receives 36 inputs and their complements from the PIM, allowing 32-bit operations to be implemented in a single pass through the chip. The wide PIM-to-logic-block interface also improves the family's routing capability.

The basic foundation of the



3. THE TWO PINOUT OPTIONS offered in the Flash370 series gives designers two macrocell options. In the versions with high I/O pin counts, all macrocells include I/O cells that tie the macrocell to one of the package pins (top block in the figure). However, in versions with a reduced pinout, half of the macrocells don't have an associated I/O cell (and related pin). Consequently, they can only be used as a buried register or as an input register for an adjacent I/O pin (lower block in the figure).

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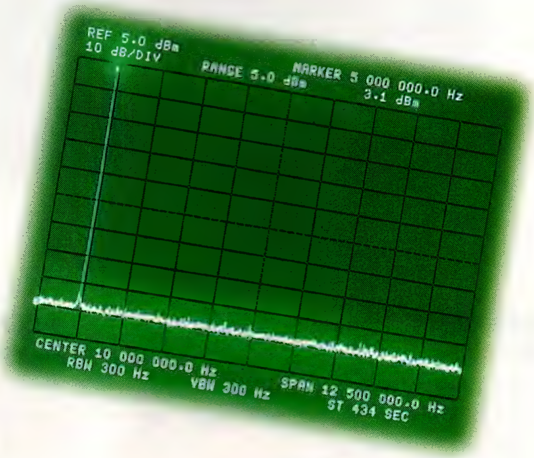

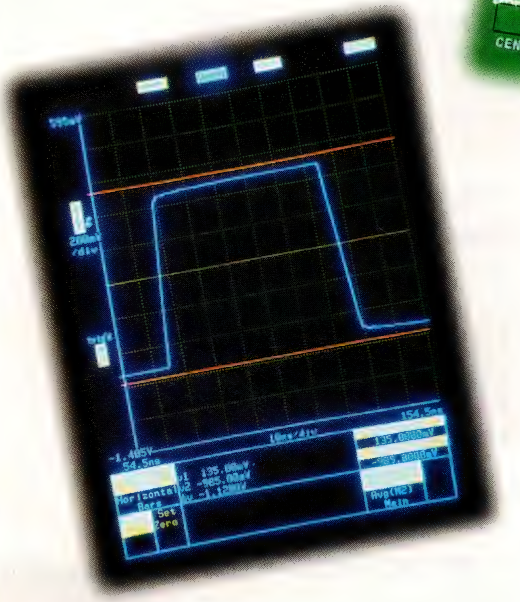

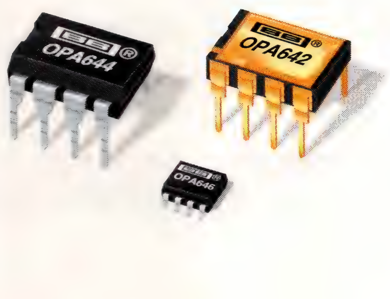

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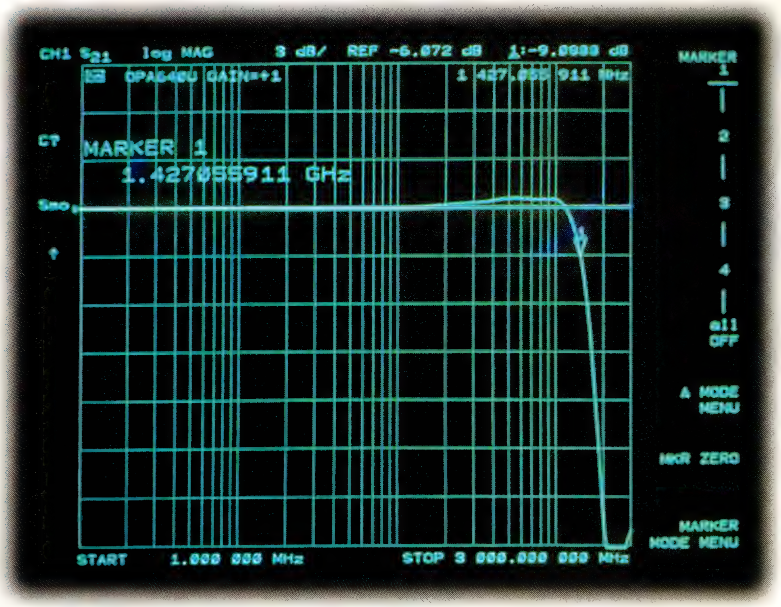

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OPA640 is the world's highest bandwidth op amp! Its speed and dynamic performance make it your best choice for critical communications and test equipment applications.

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- Low harmonics ....–82dBc at 5MHz
- High CMR.......................................85dB
- Demo board available
- Packages: 8-pin DIP, SOIC, Ceramic

1.6GHz Gain Bandwidth at G=2

OPA641 is stable in gains of two or greater and features a fully symmetrical input stage and high slew rate. Try it for RF and imaging designs.

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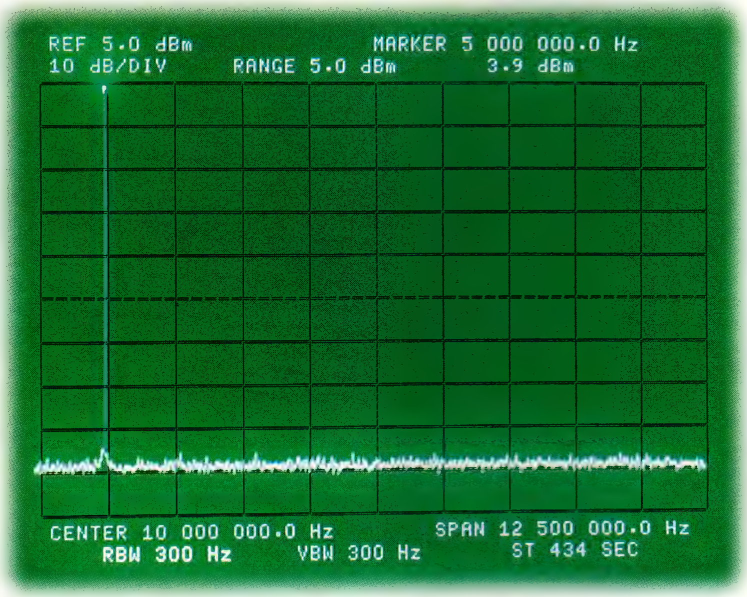

450MHz, 2.3nV/√Hz

OPA642 gives you high speed with very low distortion and noise—the right combination for your high resolution imaging applications.

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OPA642 Key Specifications

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- Low diff gain/phase error......0.006%/0.008°
- Demo board available
- Packages: 8-pin DIP, SOIC, Ceramic

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- Gain bandwidth ....1.3GHz at G=5
- Low harmonics ....–90dBc at 5MHz
- High slew rate 1000V/µs
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- Demo board available
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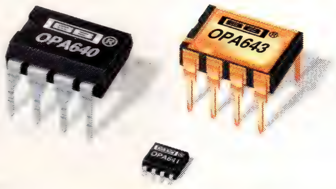

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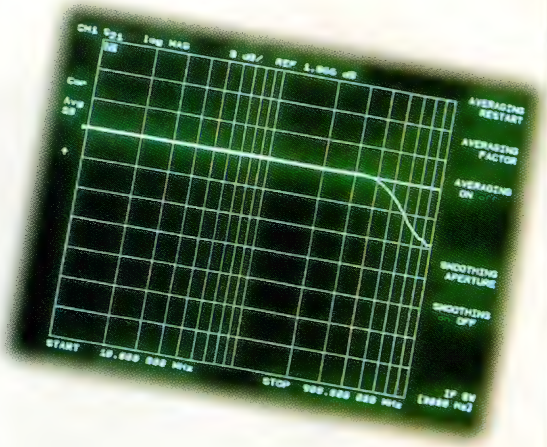
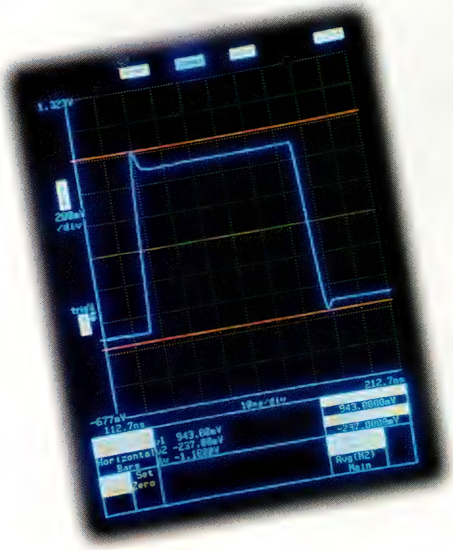
Low Power!





650MHz, 55mW

OPA646's wide bandwidth and low power simplify and improve a wide range of portable instrumentation, medical imaging, communications, and similar signal processing applications.

PLUS

OPA646 Key Specifications

- Low harmonics ....–82dBc at 5MHz, R_L = 400Ω
- Low input bias current 2μA
- Fast 12-bit settling...........15ns to 0.01%
- Demo board available
- Packages: 8-pin DIP, SOIC, Ceramic

2500V/μs, –85dBc

OPA644's current feedback design gives you very high open loop transimpedance with high slew rate and superior differential gain/phase error. It's perfect for video, RF, and other high speed signal processing uses.

PLUS

OPA644 Key Specifications

- High bandwidth 500MHz
- High open loop transimpedance 2.0MΩ
- Low differential gain/phase error ....0.008%/0.009°
- Low harmonics ....–85dBc at 5MHz
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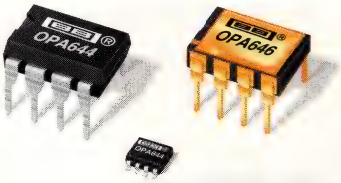
- Packages: 8-pin DIP, SOIC, Ceramic



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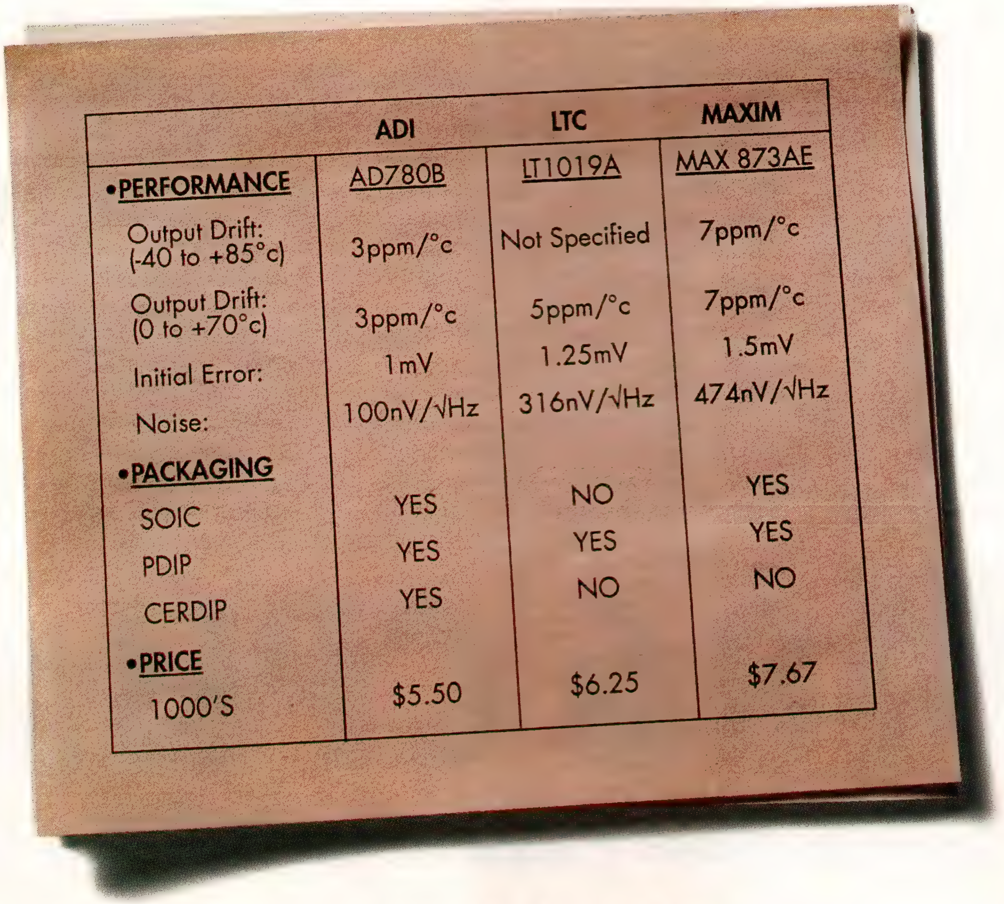
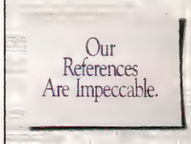


	ADI	LTC	MAXIM
•PERFORMANCE	AD780B	LT1019A	MAX 873AE
Output Drift: (-40 to +85°c)	3ppm/°c	Not Specified	7ppm/°c
Output Drift: (0 to +70°c)	3ppm/°c	5ppm/°c	7ppm/°c
Initial Error:	1mV	1.25mV	1.5mV
Noise:	100nV/√Hz	316nV/√Hz	474nV/√Hz
•PACKAGING			
SOIC	YES	NO	YES
PDIP	YES	YES	YES
CERDIP	YES	NO	NO
•PRICE			
1000'S	$5.50	$6.25	$7.67



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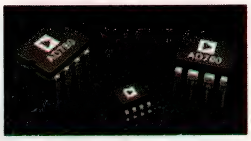

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Flash370 family is formed by the logic block that contains the 16 macrocells and their respective I/O cells. The number of I/O cells in the block for any density level depends on the packaging option—the I/O-intensive option has 16 I/O cells per logic block, while the register-intensive option has half that number.

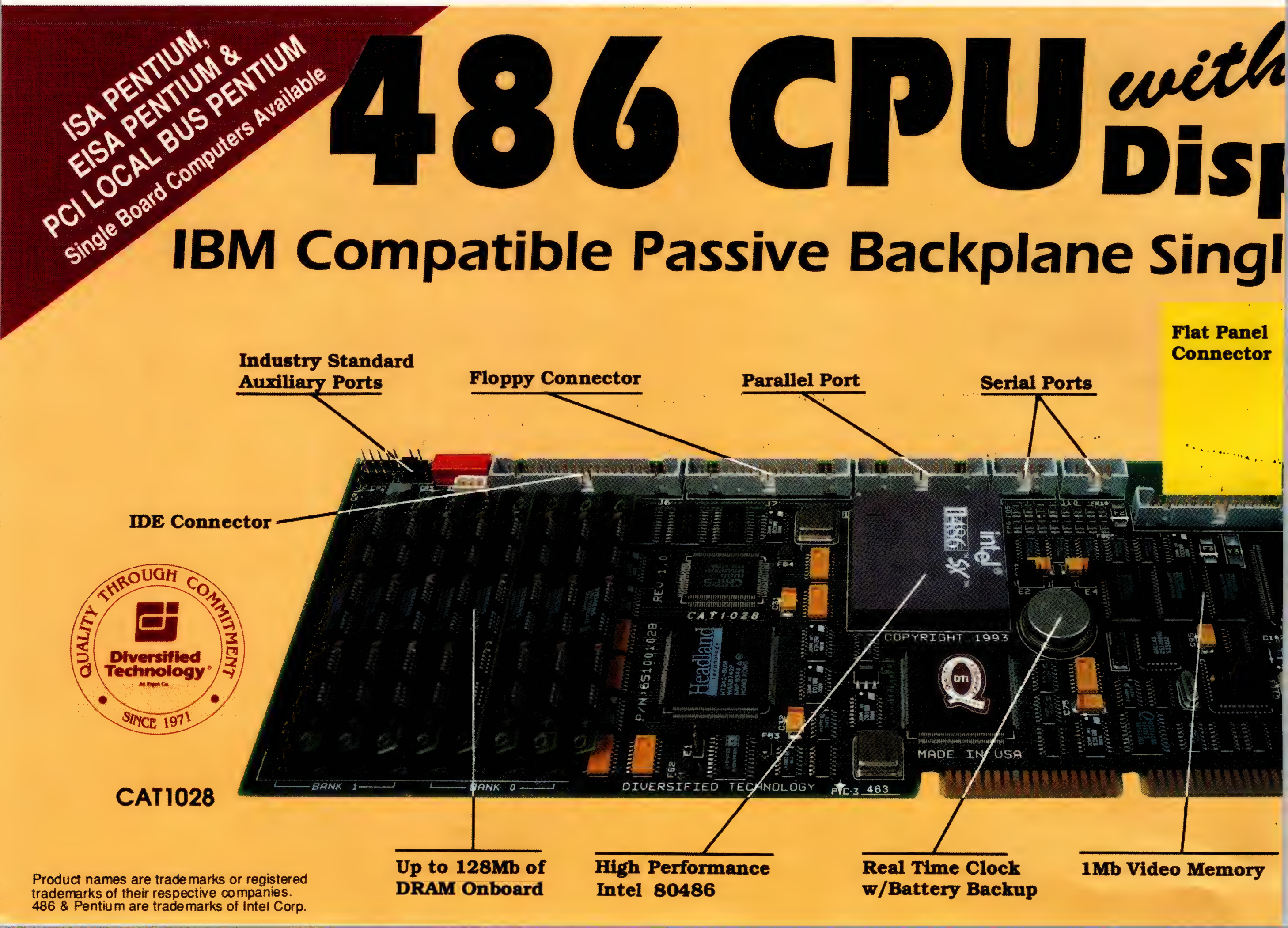
Each logic block includes a programmable 72-input-by-86-product-term array that's fed with 36 inputs from the PIM. Every PIM input originates from a macrocell feedback or an input pin. Active Low and Active High versions of each input are generated to create the full 72-line input field for the logic block. The 86 product terms in the array can be created from any of the 72 inputs. Thus, unlike other CPLDs, which are often limited in the number of inputs to the logic block (as few as 18 inputs) and in flexibility, the 36 inputs to the logic block on the Flash370 series gives designers, synthesis tools, and software support tools added flexibility. Designs thus become denser.

Although there are 86 product terms, only 80 are general-purpose—four of the remaining terms serve as Output Enable control terms, while the remaining two serve as dedicated Set and Reset product terms for all of the D/T/latch flip-flops in the macrocells contained in each logic block. Often, certain functions have unbalanced product-term requirements within a logic block. However, by allowing the software development tools to automatically distribute the product terms among the 16 macrocells, designers at Cypress have removed the headache of manually planning product-term allocation.

The product-term allocation scheme designed by Cypress includes a product-term steering capability, which is an approach that directs product terms to macrocells on an as-needed basis. For example, if one macrocell requires 10 product terms while another needs just 3, the product-term allocator will steer 10 product terms to one macrocell and 3 to another. Each product term can be individually steered and any number of terms, from 0 to 16, can be steered to any macrocell.

The product-term allocation also supports product-term sharing across multiple macrocells. For instance, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms can be shared and only have to be programmed in one product term. Sharing can be done across groups of four macrocells in an overlapping fashion. Software will automatically take advantage of this capability—the user doesn't have to intervene to figure out how best to share the terms. And neither product-term sharing nor product-term steering have any effect on the speed of a signal going from an input to an output.

Within each logic block are either 8 or 16 I/O macrocells, depending on the pinout option selected. Inside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each macrocell is a register that can be configured as a D or T flip-flop, used as a level-triggered latch, or bypassed altogether in order to employ the macrocell for combinatorial logic only *(Fig. 3)*. Registers can be asynchronously set or reset on a logic-block basis with the separate set and reset product terms. The terms can be assigned to be either Active High or Active Low, a feature that improves the efficiency of logic-synthesis tools.

Register clocking is also very flexible—as mentioned earlier, the Flash370 chips have two or four global synchronous clock inputs, any one of which can be used to clock the registers. Polarity of clocks is also programmable, permitting the registers to be triggered off the falling or rising edge of the input clock.

The macrocell output also contains a polarity-control multiplexer that can set the output as either Active High or Active Low. In addition, each macrocell has a feedback path to the PIM that's separate from the I/O-pin input path. As a result, the macrocell can be buried and the I/O pin still can be used as an input. Those family members including the dedicated buried macrocells have a cell structure that's very similar to the I/O macrocell. The only major difference is the lack of any connection to the I/O pins and the ability to serve as an input register. When configured as an input register, the macrocell gets its input from the I/O pin associated with a neighboring macrocell. All buried macrocells feed their outputs go to the PIM for final routing.

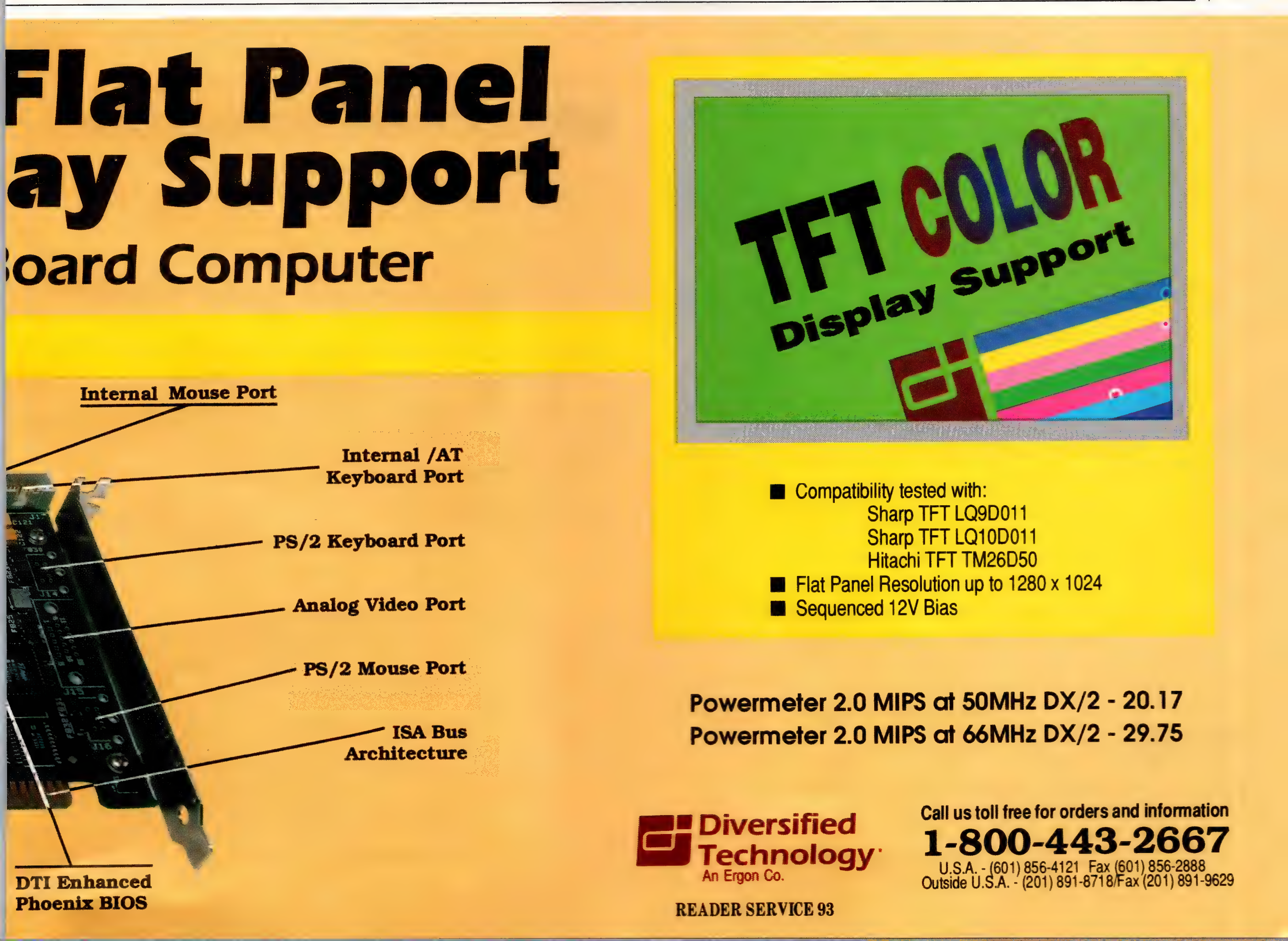
The clock/input-only pins can be configured as combinatorial, registered, double-registered, or latched. The clock polarity is also user-selectable, and the polarity is separately controllable for input and output registers. The double-register input option allows designers to configure metastable-hardened inputs, which are ideal for state machines that respond to asynchronous (external, unpredictable) events. With such hardened inputs, the machines can operate at a full-rated speed of 110 MHz, maximum, while providing a 10-year mean-time-before-metastability-failure period.☐

PRICE AND AVAILABILITY

The Flash370 family of complex PLDs includes seven initial members with I/O pin counts ranging from 32 to 256 pins. First to be sampled is the 66-MHz speed grade of the Flash371, which sells for $10.40 each in lots of 100 units. Higher-speed versions as well as the larger family members will be released throughout the year. By late 1994, the company estimates that volume pricing will come down to $6.75 or less for the 371. Samples are immediately available. Prices for the other family members will be released when the chips are sampled.

Cypress Semiconductor Corp., 3901 North First St., San Jose, CA 95134-1599; Roger Herbst, (408) 943-2798. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	530
MODERATELY	531
SLIGHTLY	532



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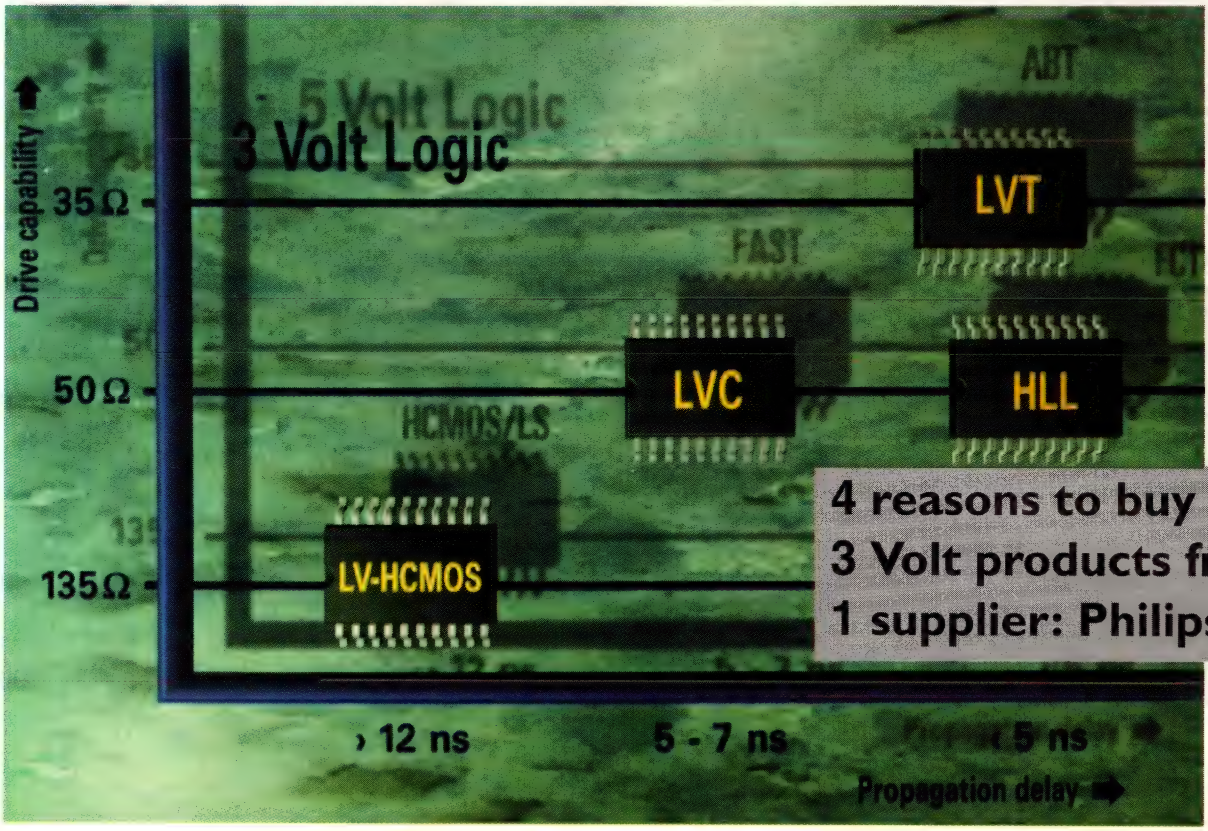

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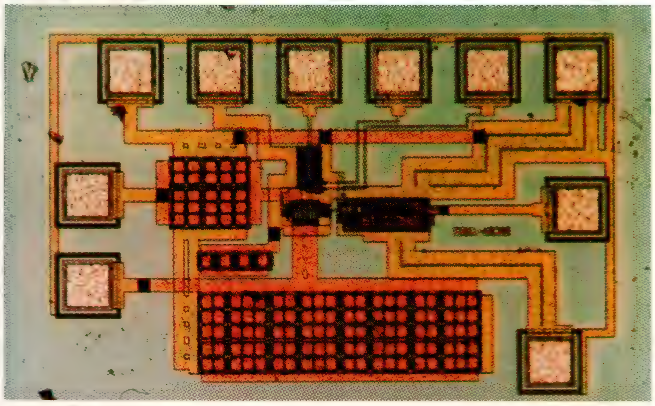
The annual International Solid State Circuits Conference (ISSCC), now in its 41st year, is *the* conference of record where virtually all IC advances are first unveiled. Such was the case at this past ISSCC, held in San Francisco, Calif., Feb. 16-18. The following four Special Reports, covering *Digital*, *Analog*, *Communications*, and *Sensor* technologies, examine in detail the development highlights in each area.

Our coverage leads off with a review of major digital-technology developments by Semiconductors Editor Dave Bursky. With chip line widths dropping down to 0.1 μm, researchers are coming up with denser and higher-performance devices, like CMOS 256-Mbit DRAMs, 64-Mbit flash memories, microprocessors with 64-bit-wide buses and throughputs of hundreds of MIPS, and low-power bipolar logic.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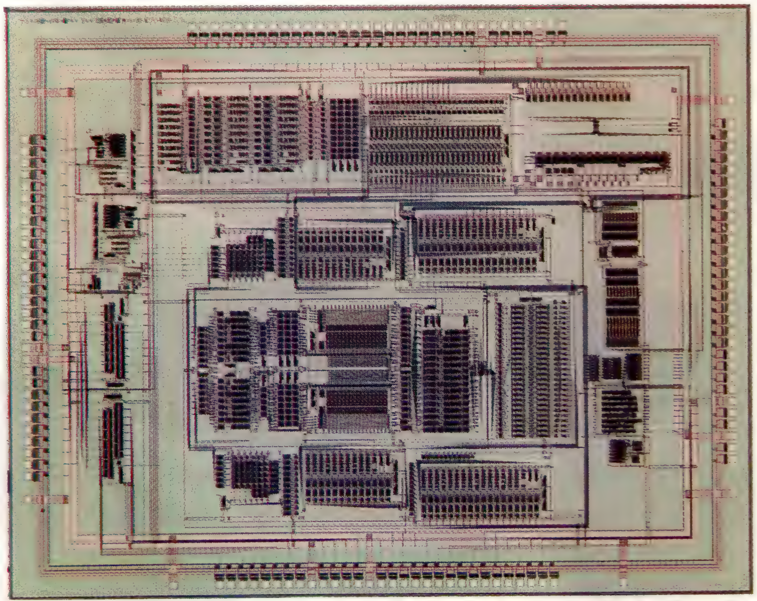
Next, Analog & Power Editor Frank Goodenough provides an overview of key analog-technology developments. Like digital ICs, the trend toward submicrometer ICs also is in full swing. Developments include a 12-bit digital-to-analog converter built from silicon germanium that offers blazingly fast 1-GHz operation. Other developments include high-speed sample-and-hold amplifiers (SHAs), including one IC that holds 192 SHAs with a bandwidth of 40 MHz and sampling at a frequency of 60 MHz.

Advanced Technology Editor Jack Shandle looks into various communications-technology developments. These are highlighted by several DSP chips with MPEG coding for HDTV that feature impressive performance levels, as well as wireless transceiver ICs which operate at multi-gigahertz rates. One such device is a 5-V bipolar chip for the 70-to-200-MHz range. It's reportedly the most integrated cellular radio IC of its kind.

Finally, Analog & Power Editor Frank Goodenough reviews developments in sensors, imagers, and displays. Highlights include a 1-MHz, full-scale, light-to-frequency sensor that handles 7 decades of light intensity, and a complete closed-loop potentiostat with an on-chip 13-bit ADC.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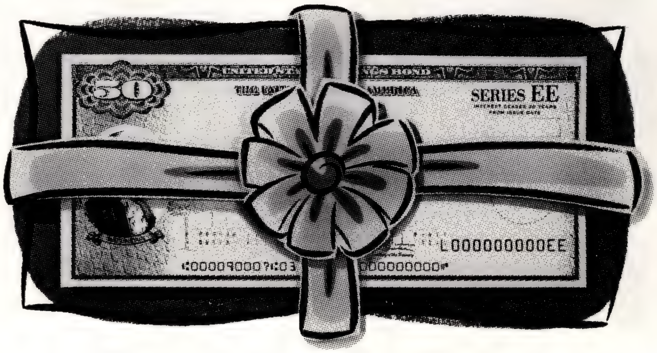

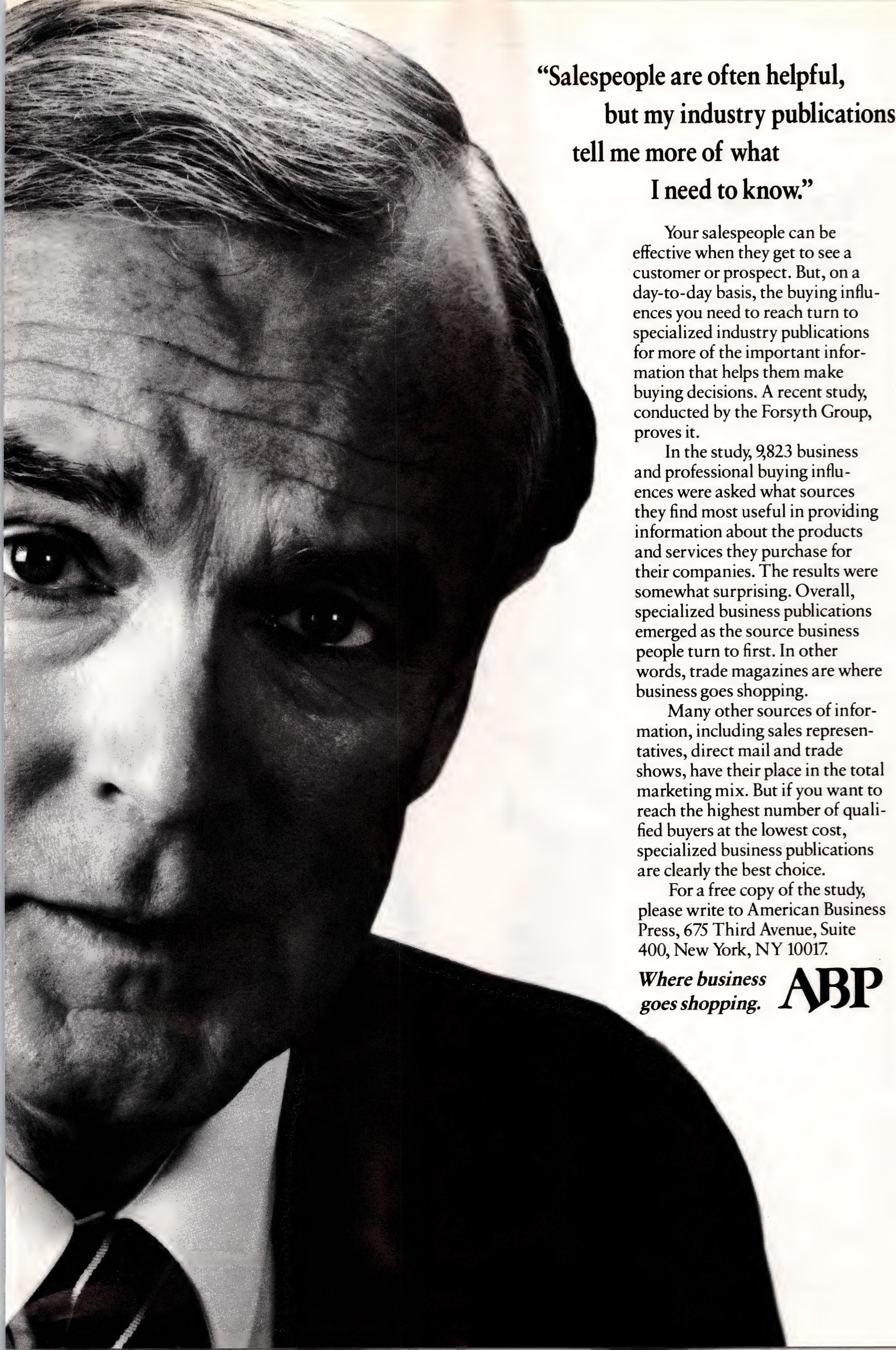

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Your salespeople can be effective when they get to see a customer or prospect. But, on a day-to-day basis, the buying influences you need to reach turn to specialized industry publications for more of the important information that helps them make buying decisions. A recent study, conducted by the Forsyth Group, proves it.

In the study, 9,823 business and professional buying influences were asked what sources they find most useful in providing information about the products and services they purchase for their companies. The results were somewhat surprising. Overall, specialized business publications emerged as the source business people turn to first. In other words, trade magazines are where business goes shopping.

Many other sources of information, including sales representatives, direct mail and trade shows, have their place in the total marketing mix. But if you want to reach the highest number of qualified buyers at the lowest cost, specialized business publications are clearly the best choice.

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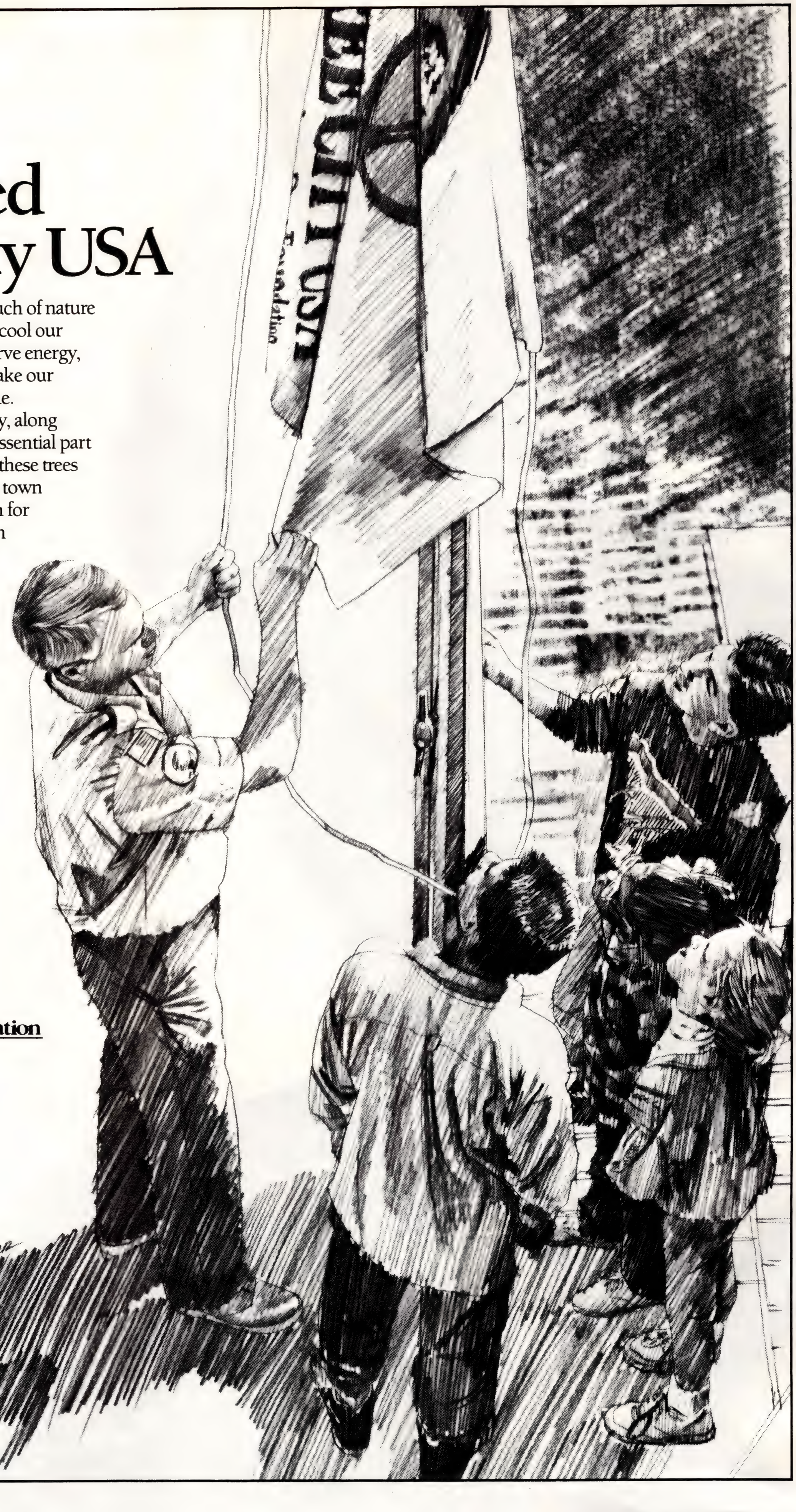


BY
DAVE
BURSKY

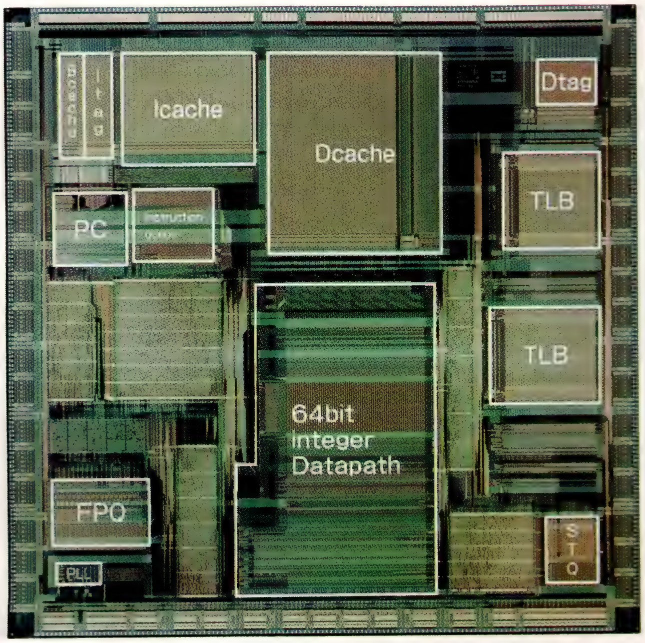
ISSCC

DIGITAL TECHNOLOGY

As expected, digital technology presentations at the International Solid-State Circuits Conference (ISSCC) continue the trend of smaller, denser, and faster ICs. For example, improvements in CMOS processing have resulted in 256-Mbit dynamic RAMs, 64-Mbit flash memories, and microprocessors with 64-bit-wide buses offering throughputs of several hundred MIPS. Among the many developments on the program were improved and scaled device structures, new nanostructures, novel quantum-flux devices, and improved neural-network circuits.

As IC-feature sizes shrink, new device structures are evolving, catapulting the next generation of circuits into the market. Many researchers, however, are trying to establish where the "final" limit is with respect to scaling: Just how small can features get before the laws of physics provide unwanted limits on the size of a single transistor?

At the University of California at Berkeley, for example, researchers examine the effects of reducing gate-oxide thickness, gate width, and power-supply voltage on CMOS circuit performance. According to their analysis, reported on in a "Technology directions: low-power technology" session, the MOSFET saturation current stops increasing as gate width drops below



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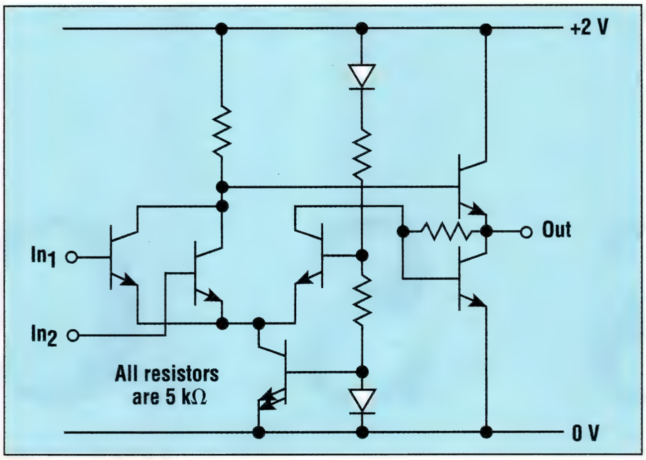
0.5 µm, due to velocity saturation and power-supply voltage reductions.

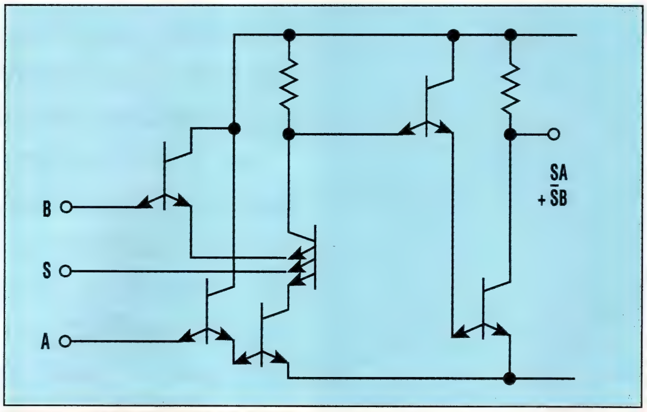


1. EMPLOYING only NPN transistors, this push-pull output NOR gate developed by Siemens uses a differential input. It can readily drive highly capacitive loads without suffering large increases in propagation delay.

The resulting speed of an inverter, they estimate, will double about every four circuit generations, as the minimum features shrink from 0.5 to 0.1 µm. Previously, it's been every two generations, from 2 down to 0.5 µm. Thus, today's unloaded inverters fabricated with 0.5-µm minimum features have a typical delay of about 100 ns, while inverters fabricated with minimum features of less than 0.13 µm will have delays ranging from 35 to 50 ps.

The researchers also expect circuits to follow two performance paths: one optimized for high speed (35 ps) and the other for low power (50 ps). The high-speed path will see the doubling stretch to every four generations, while the low-power path might require five generations to double the speed. To compensate for the slowdown in performance improvements, more pressure will be placed on the circuit designer and process developer to come up with innovative device structures and better processes.

One long-used approach for improving performance is to fabricate the circuits in an isolated silicon layer—some form of silicon on insulator (SOI). Optimized SOI MOSFETs can have higher saturation currents than bulk devices thanks to reduced circuit capacitance, lower body charge, and a small reduction in threshold voltage. Reducing the width of the metal lines that carry ac signals, such as clocks and data buses, can also help improve performance. Recent electromigration studies have shown that ac interconnects on chips can carry many times higher current densities than design rules based on dc tests would imply.



2. MULTI-EMITTER resonant tunneling hot-electron transistors can perform complex logic functions using a minimum of circuitry. With the inputs fed by common-emitter buffers, this circuit (built by Fujitsu) can be used as a data selector, implementing the output function $SA + \overline{S}B$.

Low-power, but high-performance, bipolar logic was the goal of a research effort from Siemens AG, Munich, Germany. After examining the performance losses when reduced-power emitter-coupled and current-mode logic (ECL and CML) circuits are used to drive large capacitive loads, researchers came up with a new npn-bipolar NOR gate structure. The structure, which operates at 2 V, provides the equivalent of a complementary output stage that doesn't require any change in a standard npn bipolar process *(Fig. 1)*. The strength of the new scheme is targeted as a supplement to ECL and CML circuits when driving large capacitive loads.

The output stage employs push-pull output drivers implemented with only two npn transistors. Furthermore, the circuit needs no capacitive coupling to discharge the output load. Only one of the output transistors is switched on during the transition time, thereby providing high-drive capabilities for both transitions.

The logic function in the gate is performed by a current-mode switch with a resistive load. With a 5-kΩ load resistor, the total current is 150 µA (including the bias current) when powered by a 2-V supply (0.3 mW/gate). However, due to the circuit's CMOS-like behavior, an additional power component exists that's proportional to the operating frequency and load capacitance. The small signal swing of 0.4 to 0.5 V (100 mV), though, keeps the dynamic power negligible.

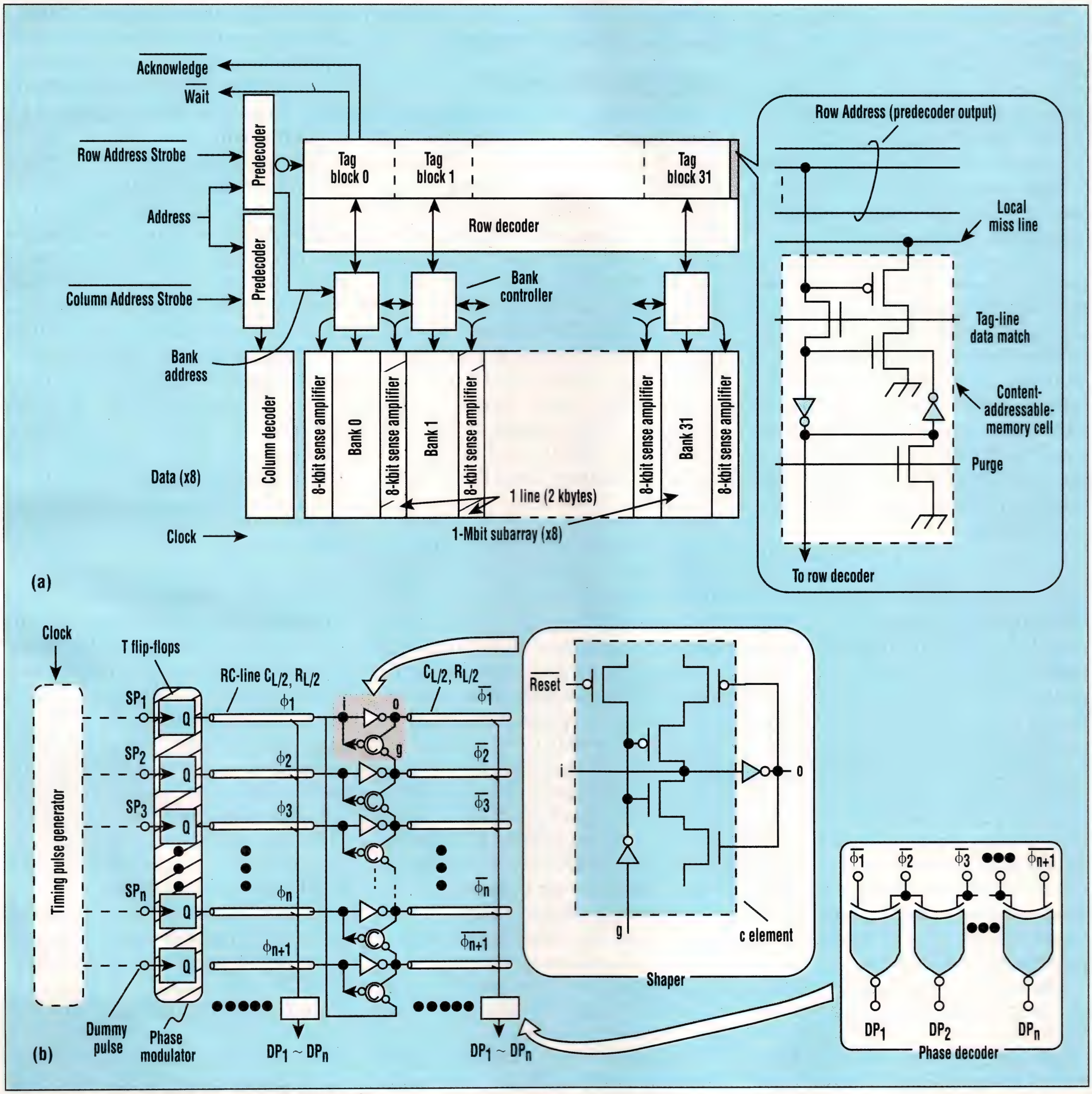
The gate propagation delay thus stays fairly constant over a wide range of load capacitances, starting at about 150 ps with no load and increasing to just 170 ps with a load of 1 pF (the equivalent of 5 mm of metal). The resulting speed-power product of the gate is about 0.1 pJ—a factor of 3 to 10 lower than with direct-coupled FET logic implemented in gallium arsenide (GaAs) or biCMOS NAND gates operating at 100 MHz. More complex functions such as flip-flops can be implemented with 2-level series-gating operating in a differential mode.

Although dimensions of 0.1 µm are considered exceptionally small by today's standards, there's still a smaller world where operations are performed by the movement or manipulation of a single atom or electron. In the "Technology directions: nanoelectronics, superconductivity, and optics" session, Fujitsu Laboratories Ltd., Atsugi, Japan, examines various techniques, including ballistic electron motion, electron-wave interference, single-electron tunneling, and quantum-effect switching circuits. Some of these technologies look promising for the creation of gigabit-density memories, but many of them must still be developed further.

In the same session, Fujitsu discusses high-density logic circuits using multi-emitter resonant-tunneling hot-electron transistors (RHETs). The devices are fabricated in indium-GaAs (InGaAs) and operate at 77K. Combining logic functions into a multi-emitter transistor allows for more compact circuits, which in turn reduces cross-chip wiring delays. The net result is improved circuit performance and lower power consumption.

The multi-emitter structure contains separate emitters and emitter barriers but shares a common base, collector barrier, and collector. The transistor turns on when the maximum potential difference among the emitters exceeds a certain threshold voltage—the sum of the emitter barrier's forward and reverse turn-on voltages. When the transistor turns on, electrons in the low-potential emitter are injected into the base layer. Most electrons surmount the collector barrier and reach the collector electrode.

The electrons scattered in the base region pass through the emitter bar-



3. CACHE AND TAG MEMORIES are combined onto the DRAM along with 256 Mbits of main storage in this memory architecture developed by Oki (a). As a result, each of 32 memory banks has its own 16 kbits of cache and a 20-bit content-addressable memory for tag references (a). To keep the timing very precise, the DRAM's designers created a precision pulse-transmission generator that works with a phase modulator, a signal shaper, and a phase decoder (b).

rier and reach the high-potential emitter electrode, which acts as a sink for scattered electrons, similar to the base electrode in a conventional (single-emitter) RHET. The emitter electrodes thus act as both an emitter and a base, depending on their potentials. As a result, a simple three-emitter RHET with a resistor in series with the collector can implement a function like $ABC + \overline{A}\,\overline{B}\,\overline{C}$—an AND/NOR gate.

For instance, by connecting one emitter to a pull-down (current-sink) input (A), another to a pull-up (current source) input (B), and the remaining emitter to a voltage source (S), the RHET can turn off on two conditions: when the voltage source is high and the pull-down input is low, or when the voltage source is low and the pull-up input is low.

This type of function would serve well as a noninverted data selector that would implement a function such as $SA + \overline{S}B$ *(Fig. 2)*. The multiemitter elements can also be used to implement flip-flops and static-RAM cells. Emitter followers must be added to the inputs to help set the desired threshold level. The transistor can also perform other useful functions simply by adding further external elements.

Just as the RHET structures are expected to operate well into the gigahertz range, a new logic technology proposed by Hypres Inc., Elmsford, N.Y., will allow operation in the tens of gigahertz with just a few microwatts of power dissipation. Based on a novel superconductive, rapid, single-flux quantum technology, the Hypres scheme takes full advantage of the fundamental properties of superconductivity. The structures are implemented on the company's 10-level niobium/aluminum oxide/niobium thin-film process. They employ minimum Josephson-junction sizes of 3.5 by 3.5 μm and 2-μm minimum line widths.

Data and clock signals are picosecond-long quantized voltage pulses that correspond to the transfer of single magnetic-flux quanta. These pulses are regenerated at each gate and processed by circuits consisting of overdamped Josephson junctions interconnected via microstrip inductances. The inherent internal memory of all rapid single-flux quantum gates (primarily flip-flops) combined with their high switching speed makes them appealing for low-circuit-area serial, bit-pipelined architectures. Experimental circuits implemented with the technology demonstrate operating frequencies of up to 60 GHz for a 4-bit shift register, 120 GHz for a 12-bit counter, and 6.3 GHz for an N-by-8-bit multiplier. As of yet, these are some of the highest operating speeds reached, and that spans across all technologies.

DRAMs AND SOI

Most practical applications of these emerging technologies are at least 5 to 10 years away, but some aspects are already starting to appear. An experimental 64-kbit DRAM fabricated with SOI structures, jointly developed by Mitsubishi Electric Corp. Ltd., and Daioh Electric Co., both in Itami, Japan, is unveiled in the "DRAM and non-volatile memories" session. The DRAM offers a wide operating voltage range and a long storage time thanks to the separation by implanted oxygen (SIMOX) SOI process. It lets chip designers place the memory cells in a 100-nm-thick isolated film of silicon.

Longer storage time is an important factor, especially if the DRAMs are to operate at very low supply voltages, such as 1.5 V. Mitsubishi designers estimate that using SOI reduces the bit-line capacitance by about 25%. As a result, a memory cell implemented as part of a 256-Mbit array should be able to retain data for at least 5 seconds at 80°C. Such a storage capability can be achieved with a cell capacitance of just 4.5 fF. In contrast, a bulk-based DRAM would require about 24 fF. Placing the capacitor in the SOI layer reduces leakage considerably, which means the capacitor can be much smaller—just 7.5% the size of the bulk capacitor.

The small cell size possible with SOI technology will eventually lead to gigabit-generation DRAMs. These must have extremely small memory cells to fit on reasonably sized chips. In the meantime, more down-to-earth developments are leading to functional 256-Mbit DRAMs, which were also described in the same session. A trio of Japanese-manufactured 256-Mbit memories, one each from Mitsubishi; Matsushita Electric Industrial Co. Ltd., Osaka; and Oki Electric Industry Co. Ltd., Hachioji; show three different approaches to achieve high-performance levels.

Mitsubishi's designers use a boosted sense-ground scheme. It extends the data-retention time of a 32-Mword-by-8-bit DRAM that accesses in 34 ns. The three-level-metal 0.25-μm process employed provides a cell capacitance of 25 fF in an area covering just 0.72 μm^2. An external 3.3-V power supply is down-regulated to 2.5 V internally.

Packaging also received a great deal of attention by Mitsubishi engineers. Instead of mounting the chip in a package, a chip-scale package was developed. First, contact electrode "pillars" instead of bonding pads are placed on the memory chip itself, and then plastic resin is molded around the chip to a thickness just slightly lower than the cylindrical pillars. Consequently, the ends of the pillars can slightly protrude from the plastic, forming contacts to the rest of the system. Because such a package is much smaller than its traditional counterparts, it allows the chips to be mounted closer together and be used in systems with thinner profiles (e.g., memory cards).

Combining cache and tag memories on the same chip as the main memory, Oki's 256-Mbit DRAM can deliver data at 125 Mbytes/s. Divided into 32 banks, the 32-Mword-by-8-bit device includes sense-amplifier cache strips and the associated tag memory embedded in the row decoders to form a distributed cache. In addition, an on-chip bank-interleaving scheme provides short access times to data held in the 32 banks.

In the DRAM, which is powered externally by a 2.4-V supply that's internally downregulated to 1.5 V, a total of 33 sense-amplifier strips, each containing 8192 amplifiers, are laid out to sandwich their associated banks *(Fig. 3a)*. Each bank has one tag block consisting of 20 content-addressable memory (CAM) cells. The cells hold both the previously accessed word line address and that of the activated, associated sense-am-

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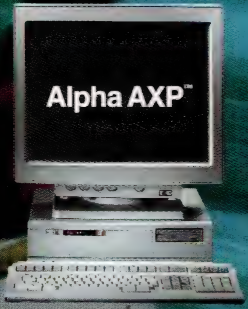

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plifier strips.

The memory's synchronous operation starts when the Row Address Strobe (RAS) decoder output is enabled and selects one of the 32 banks, the related bank controller, and the tag block. The tag block tests the address for a cache hit with the previously latched CAM data. Depending on a hit or miss, the circuit does one of three operations: it reads the data from the cache; it indicates a bank hit and must load data from the bank into the cache; or it indicates a cache miss, requiring a full memory cycle to load the cache.

The cache latency varies depending on the mode—3 clocks for a cache hit, 4 clocks for a bank hit, and 7 clocks for a cache miss (8 ns/clock). During a cache miss, the Row Address decoding continues as usual and the tag block latches the new RAS pre-decoder output for a possible future cache hit. For every read/write/refresh operation, two 8-kbit sense-amplifier strips, one on each side of a bank, are activated (they provide the equivalent of a 2-kbyte cache line).

One concern with the tight synchronous timing required by the cache-DRAM scheme is having to transmit extremely narrow control pulses at precise time intervals and at very high rates. The solution is a pulse-transmission scheme that uses Exclusive-OR gates between consecutive multi-phase signals to compensate for time lags that are caused by the line-transmission characteristics *(Fig. 3b)*.

The signals are generated with three key circuit subsections—a phase modulator, a shaper, and a phase decoder. The phase modulator is basically a string of T flip-flops and receives various control pulses at different timing points. Signals produced by the modulator propagate down the RC-loaded transmission paths. Each signal encounters a shaper circuit in the middle of the path to restore it to its proper shape. Selecting the proper signal is the task of the phase decoder, which routes the signals to the right bank-control input.

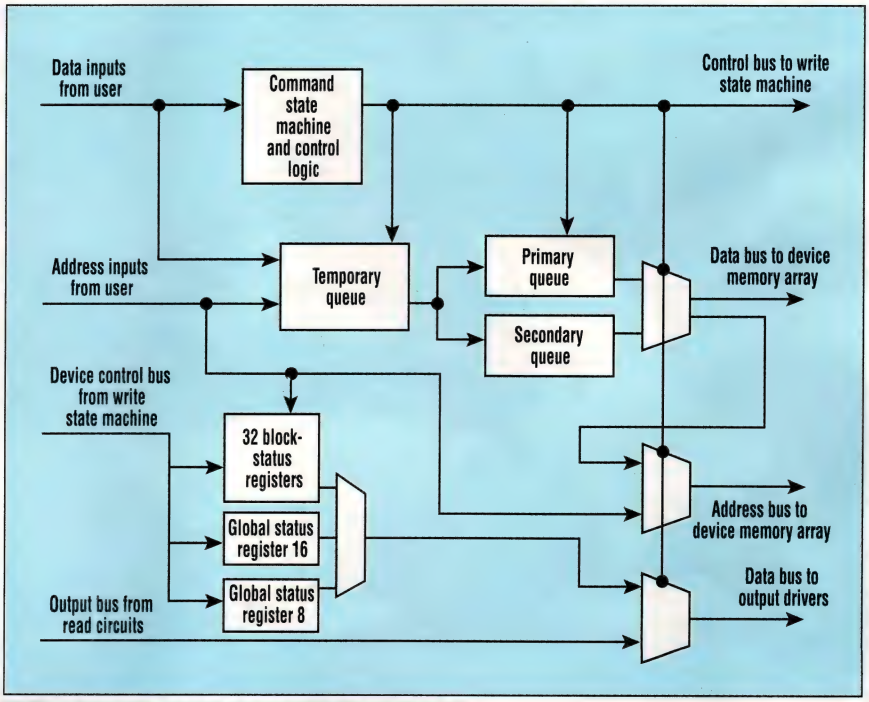
DRAMs Hold Video

The same session also delves into high-density DRAMs for storing motion video. Designers at Matsushita estimate that a single 256-Mbit chip can hold about 171 seconds of NTSC video data if encoded with the MPEG-1 algorithm. Optimizing the memory's architecture for motion video allowed them to create a memory that transfers data at 100 MHz through 16-bit parallel ports (10 ns/transfer). The dual ports give the chip an effective bandwidth data rate of 1.6 Gbits/s, making it possible for the memory to handle the data rates required by high-definition TV as well.

The chip can read through all memory locations in about 168 ms. About 128 ms is required to refresh the chip. Consequently, the refresh operation must be incorporated into the memory during full bit-read and -write operations to ensure that all locations are refreshed. To do that, a self-refresh mode that functions during serial-transfer operations is included. Each of the eight 32-Mbit arrays contains its own refresh counter, an address multiplexer, and a shift register. Therefore, seven of the eight memory banks (those not selected) perform refresh operations during each memory access cycle.

Internally, the memory is designed to operate from a 2.5-V supply. Most of the internal circuits, however, operate from a reduced voltage level of 0.6 V to minimize the stress imposed on the 0.25-μm minimum features. The 0.6-V supply is used by the circuits that employ a suppressed high-level differential transfer (SHT) scheme implemented with NMOS transistors (due to their larger g_m). The SHT scheme, which reduces the operating current by almost 17 mA versus a standard transfer circuit, is about 3.5 ns faster than conventional approaches. On the receiver side, the SHT circuit starts with PMOS input devices and an NMOS cross-coupled amplifier.

From the realm of volatile data storage, papers in the same session switch to nonvolatile flash-storage technology, with three presentations that describe 16- and 64-Mbit chips. The largest of the trio is a 64-Mbit chip developed by NEC Corp., Tokyo, Japan, which operates from a 3.3-V supply. The 4-Mword-by-16-bit memory includes a dynamic bit-line latch-programming scheme that keeps the access time to 50 ns and allows erasure/programming in blocks as small as 256 bits.


Data inputs from user
Command state machine and control logic
Control bus to write state machine
Address inputs from user
Temporary queue
Primary queue
Secondary queue
Data bus to device memory array
Device control bus from write state machine
32 block-status registers
Global status register 16
Global status register 8
Address bus to device memory array
Data bus to output drivers
Output bus from read circuits

4. UP TO THREE INSTRUCTIONS can be queued by this 16-Mbit flash memory created by Intel. Its write operations are controlled by a small 16-bit programmable state machine that can easily be modified as new programming algorithms are developed.

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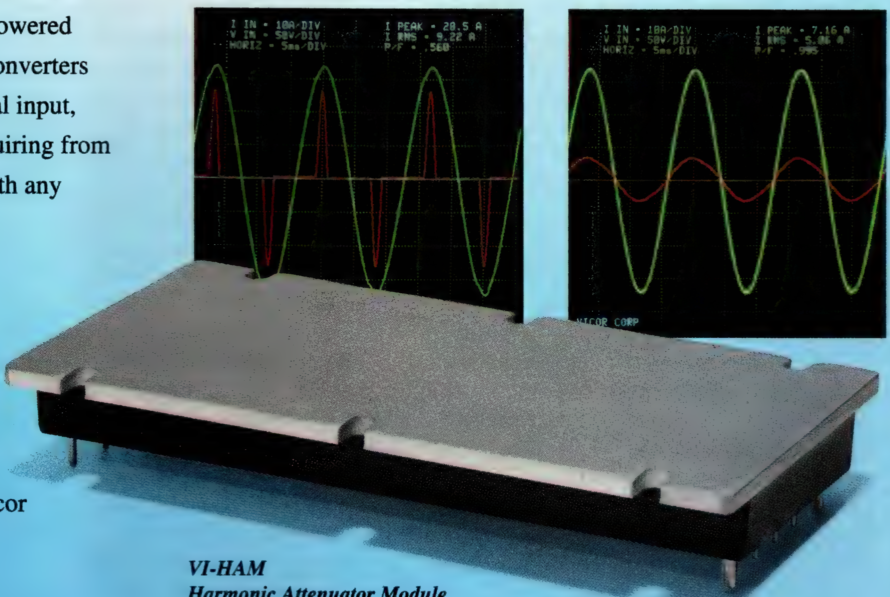

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In the dynamic bit-line programming scheme, many bits are programmed in one cycle without limiting the internal data-bus width. The bit lines are used as dynamic latches, holding the incoming data bits. The programming bit-line voltages must be refreshed once every 16 cycles because the bit-line charge is reduced by the programming current.

Programming is performed in a maximum of 10 cycles of 100 μs each. A program-verify function is executed for each 16-bit word (repeated 16 times for the 256-bit block). After the first 16-bit programming cycle, the data from the 16 cells connected to the same sub-word line are read and compared with the data in the data registers. If the data are the same, the data registers are rewritten so the chip doesn't program the bits over again. Because the program-verify unit capacity is small (16 bits), overprogramming can be avoided, thus extending memory life.

Designers at Intel Corp., Folsom, Calif., took a different approach to flash-memory architecture by crafting a 16-Mbit chip that can operate with either a 3.3- or 5-V supply. Described in the same session, it offers either a 16-bit-wide or an 8-bit-wide data organization. When the chip switches to the 3.3-V mode, a word-line boost circuit is enabled, the input-buffer trip points are modified, and the read-path circuits are reconfigured for optimum performance. However, for programming, the flash memory requires a 12-V external supply. The memory array is divided into a total of 32 blocks, providing the smallest rewritable block with a capacity of 512 kbits.

The chip incorporates a unique user interface that permits the host to queue up to three commands for execution by the on-chip write-state-machine block *(Fig. 4)*. The state machine can also be interrupted from its write sequence if a read request comes along. After the read request is serviced, the state machine continues its write operation.

Rather than use dedicated logic for the state machine, Intel's designers opted to implement it as a programmable controller with a 16-bit ALU, a triple-ported 16-word-by-16-bit register file, a 2-kword-by-19-bit instruction code array, and a program counter that supports one level of interrupt and four levels of call/return. By making it programmable, designers can easily modify the chip operation if a better control algorithm is developed. An internal clock cycles the state machine at 9 MHz, with each instruction executing in one clock cycle.

The same session also reported on ways to enhance chip yields of a 16-Mbit flash memory. Mitsubishi's designers describe how they applied Gray code to the row decoder. This allowed programming before erasure to the defective word lines without incurring a chip-area penalty. Using a Gray code also helps avoid overerasure, because many cells can be programmed before a full-erasure programming cycle takes place, reducing the number of times a cell gets programmed. Such a scheme invokes no area penalty in the row decoder as well as no architectural design restrictions.

Just emerging from research laboratories are nonvolatile memories based on ferroelectric capacitor cells. Such memories offer potential lifetimes five or six orders of magnitude longer than flash-type technology, and much shorter cell-programming times. In one example, Matsushita Electronics Corp., Kyoto, Japan, and Symetrix Corp., Colorado Springs, Colo., describe a 256-kbit nonvolatile memory implemented with ferroelectic capacitors in the "Technology directions: memory and packaging" session. It uses a one-transistor/one-capacitor cell structure—about half the number of elements as that of other reported ferroelectric nonvolatile memories.

The nonvolatile memory can operate at 3 V and reads or writes its contents at 100 ns. It can also operate in a reduced-power mode, consuming just 3 mA with a 200-ns cycle time. The cell's DRAM-like simplicity will allow very-small-area chips or very-high-capacity memories to be readily implemented over the next few years. Such a belief is held by Micron Semiconductor Inc., Boise, Idaho, which in the same session presents a study of ferroelectic progress. It concludes that the time is right to continue research to eliminate film fatigue and significantly improve aging and imprint resistance.

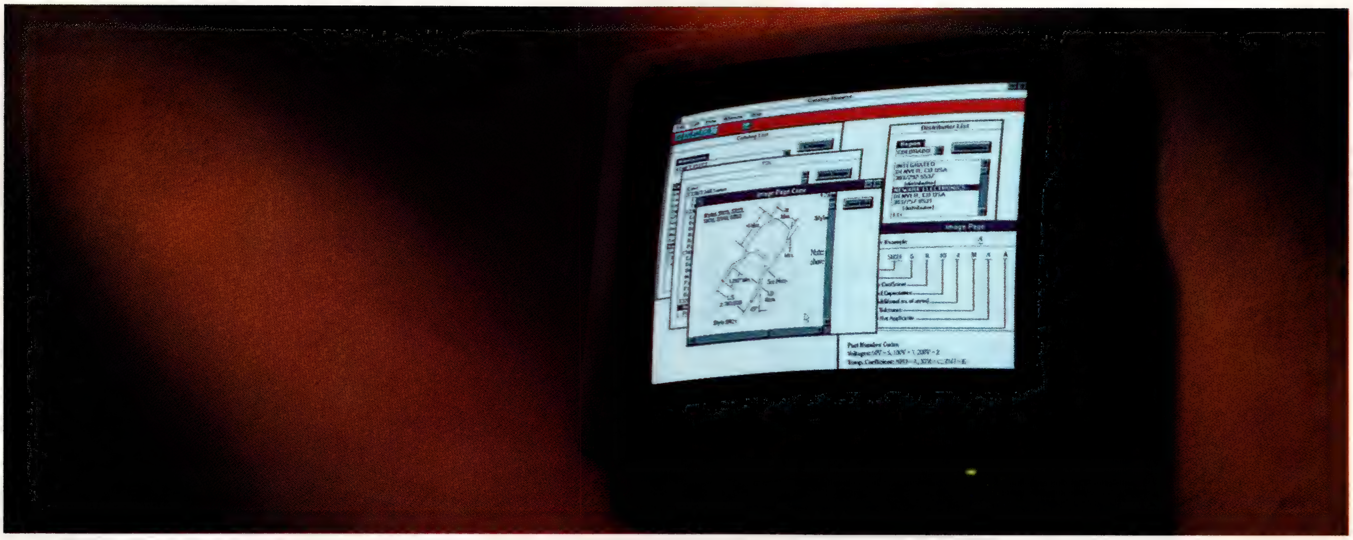
Static-RAM representation was fairly slim at this year's conference—only two papers were submitted in the "Static memory for high-bandwidth systems" session. Employing a biCMOS process, designers at NEC describe a 16-Mbit synchronous SRAM that uses a 2-stage wave-pipelining scheme to achieve fully random data-access rates of 220 MHz. Organized as four 512-kword-by-8-bit asynchronous memory blocks, the SRAM has its data path divided into several pipeline stages. To do that, each memory block is made fully static by using bipolar sensing circuits. These sensing devices operate with small voltage swings and don't require clocked equalization.

At certain points in time, two signals exist simultaneously on the data path, forming a sort of pipeline. Because the data-path lengths vary depending on the location of individual memory cells, the wave has a time range. Output signals must be acquired during non-wave periods. Stable wave-pipeline operations require a reduced time-region width. To do that, the variation in delay times from the asynchronous SRAM blocks must be minimized. Most of the delay variation comes from wiring delays, which forced NEC's designers to come up with a new wiring architecture.

VIRTUAL PORTS EASE DESIGN

Designers at IBM Corp., Essex Junction, Vt., describe a virtual three-port memory array that can access three times in a 66-MHz bus cycle. The array, which implements a super-fast memory cell, keeps the design of the core cells very simple, minimizing area occupied by the memory array. Internally, the single-ported SRAM core operates at 200 MHz; the surrounding logic controls the access to the 64-kbyte memory array. That array is organized internally as four banks of 4 kwords by 36 bits. Any location can be accessed through two read/write ports and one write-only port.

Externally, the memory appears as a 36-bit-wide RAM to the host system, a 2-kword-by-288-bit read mem-



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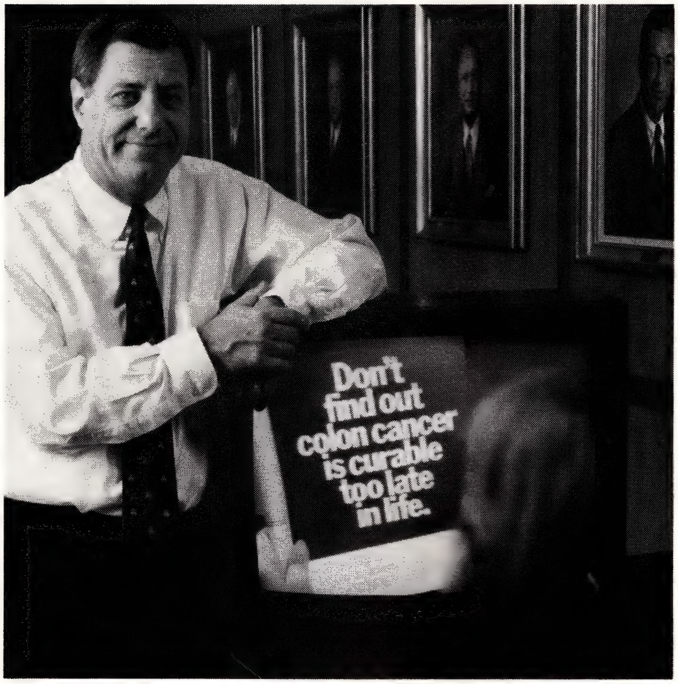
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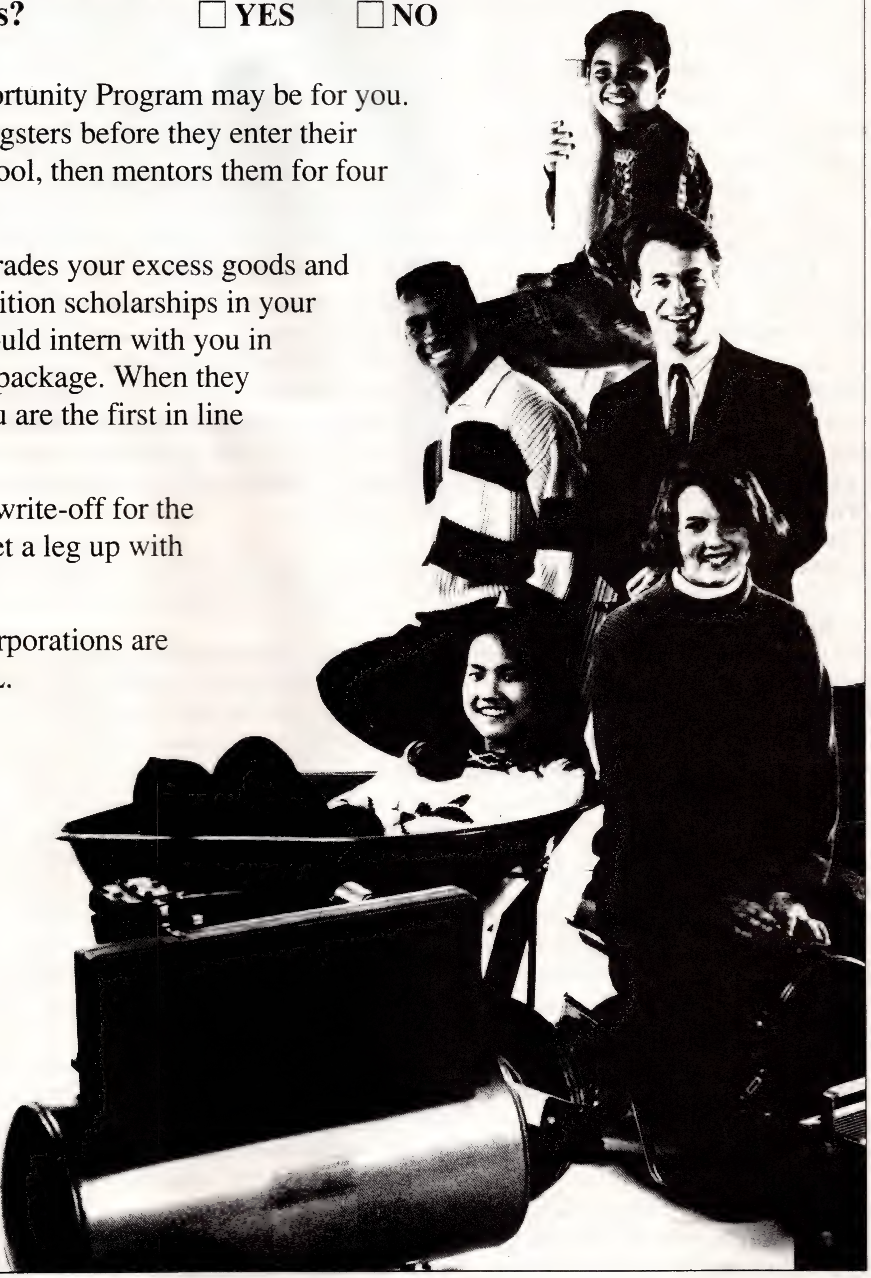


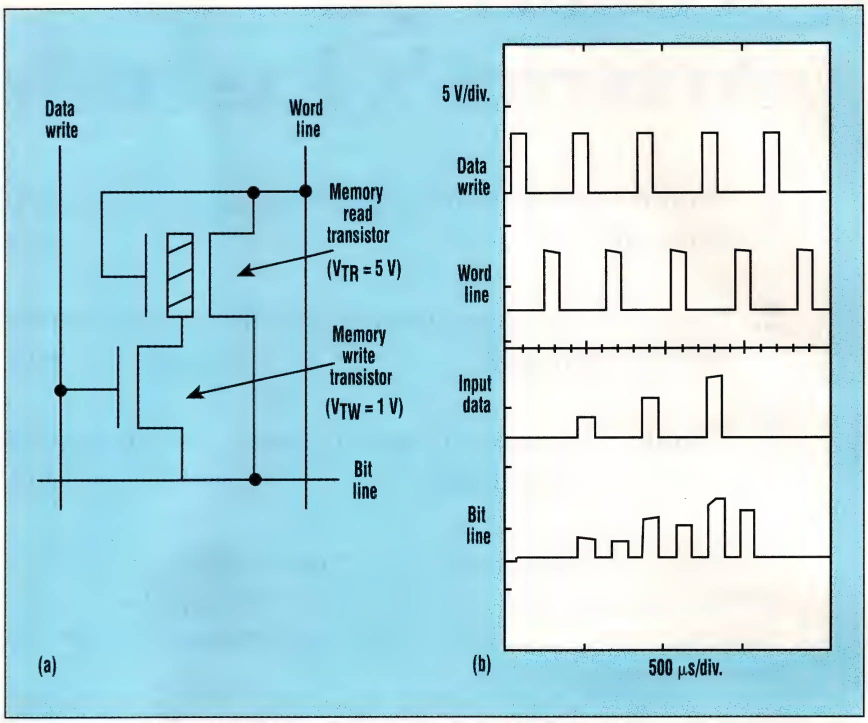
ory (or storeback buffer), and an 8-kword-by-72-bit memory-write interface (reload buffer). The memory can perform cache-line zeroing, port prioritization, address-compare bypassing, byte alignment, and four-way set associativity. It also includes built-in self-test logic.

High-density memories are key components for forthcoming high-end computer systems based on advanced 32- and 64-bit microprocessors, like those described in the "Microprocessors" session. Probably the highest-profile presentation in the session is the lead paper by Intel Corp., Hillsboro, Ore., which details the improvements the company made on its Pentium microprocessor.

By pushing the internal clock speed up to 100 MHz, the processor can deliver a peak throughput of 100 SPECint while dissipating about 8 W—about half the power of the previous-released first-generation Pentium. To get that performance improvement, a fourth level of metal is added to reduce interconnection delays and improve packing density, thereby shrinking chip area. Additional clocking schemes are incorporated to support fractional bus-to-core clock ratios and selective power-down capabilities.

The joint efforts of Toshiba Corp., Kawasaki, Japan, and Silicon Graphics Computer Systems Inc., Mountain View, Calif., sparked the creation of a CMOS superscalar microprocessor described in the same session. This single chip provides more computational throughput than a Cray 1 supercomputer—300 MIPS and 300 MFLOPS. Although first unveiled in early 1993, few details of the 64-bit architecture with its four-issue superscalar pipeline have emerged until now. The processor, which employs about 2.6 million transistors, can execute up to four instructions per cycle. Thus, when running at 75 MHz, it delivers the 300-MIPS peak throughput.

To support the high throughput, its designers put 16-kbyte data and instruction caches on the chip. And, to ensure fast branches, the chip includes a 1024-entry branch cache for branch prediction and a 384-entry 3-way set-associative translation look-aside buffer (TLB). The TLB is also dual-ported so that it can support two independent memory instructions per cycle.



5. A NOVEL MEMORY CELL THAT DIRECTLY stores the bit-line voltage on the floating gate of the read transistor was designed at Tohoku University (a). The cell, based on a previously-developed structure dubbed the Neuron MOS transistor, can store the bit-line voltages and then read them back by placing a voltage equal to the read transistor's threshold voltage on the word line. That places the read transistor into a source-follower configuration and causes the voltage on the bit line to match that of the stored value on the gate (b). Furthermore, the gate doesn't lose its charge. Consequently, its value doesn't require rewriting, as is the case in other memories such as DRAMs that have a destructive readout.

The integer portion of the CPU implements a five-stage pipeline that includes two ALUs, one barrel shifter, a multiply/divide unit, and a 13-port (9 read, 4 write) register file used to hold all temporary data. A memory-function unit includes two adders to compute the virtual addresses, two load data aligners, one store data aligner, a data cache, and the TLB. The separate floating-point unit (FPU) is fed by two 64-bit-wide banks of external cache. The cache can range from 1 to 16 Mbytes.

Yet another processor from the MIPS Technologies Div. of Silicon Graphics, the R4200, is also detailed in the same session. Designed for low-power systems, the chip takes full advantage of a 0.64-µm CMOS process and a 3.3-V supply to trim operating power to less than 2 W at 80 MHz internally (40 MHz externally). To reduce power, a very modular logic design was used in the chip, especially in the state machines. The state machines were subdivided into still smaller units, each having a dedicated function. When their functions aren't needed, these state machines become idle by default and consume little dynamic power.

Continuing in this session, designers at IBM describe what they did to spruce up the licensed 80386 architecture. Their efforts produced a 66-MHz, 32-bit, 386-instruction-compatible processor that delivers 26 MIPS and dissipates just 1.77 W at maximum speed. To reduce the power, the chip employs a 16-bit data interface to the host system and a 24-bit address bus. To keep the internal performance high, though, the processor includes a 16-kbyte, 4-way set-associative cache and a clock doubler that allows the external bus to operate at 33 MHz when the chip runs at 66 MHz internally. Optimized for 3.3-

V operation, the chip also includes several power-saving modes that are enabled by special machine-specific registers.

Many of the same power-saving techniques were applied to the PowerPC family, as detailed by designers from the IBM Somerset Design Center, Austin, Texas. Specifically, they talk about the 75 SPECint/85 SPECfp superscalar RISC processor, the PowerPC603, released late last year. Fabricated with 0.5-µm design rules and four layers of metal to keep the chip area and internal delays small, the chip can be clocked at up to 80 MHz internally, yet it dissipates just 3.3 W, maximum, from a 3.3-V supply.

Two levels of power management were incorporated. First, power drain was reduced during normal operation thanks to dynamic power-management logic. Second, three selectable static power-management modes were incorporated to trim power during periods of processor inactivity. Dynamic power-management logic determines on a cycle by cycle basis if a particular logic block is needed during that cycle for instruction execution. If not needed, the block is disabled and powered down to minimize active power.

Showing off its highest performance PA-RISC family member to date, designers at Hewlett-Packard Co., Cupertino, Calif., present the inner workings of the company's latest 140-MHz 64-bit processor. The processor includes a 64-entry (2-kbyte) fully associative prefetch/miss cache that helps reduce the effective cache-miss latency. Dual ALUs in the chip's integer data path allow the processor to perform integer-integer superscalar execution, while single-cycle load/store operations are possible to large off-chip instruction and data caches.

Using a 120-MHz, 64-bit multiprocessor system bus interface, multiple CPU modules can be tightly coupled to memory and I/O subsystems without any external components, simplifying the design of multiprocessor systems. The processor includes an on-chip FPU that can perform single- and double-precision computations. Furthermore, the chip includes a fully associative, unified TLB with 120 fixed-size entries and 16 variable-size entries to minimize overheads during address translation.

The speed crown at this year's conference is taken by a bare-bones 32-bit RISC CPU that operates at 500 MHz. Developed by NEC, it's implemented in a 0.4-µm CMOS process. The CPU uses an 8-stage pipeline and two double-stage pipelined 1-kbyte caches for both instructions and data, a 32-bit double-stage pipelined adder, and a barrel shifter. An on-chip phase-locked-loop clock generator multiplies the input clock by 2, 4, or 8 to obtain the 500-MHz internal clock. The eight-stage pipeline consists of two instruction-fetch stages, a register-file fetch and instruction decode stage, two execution stages, two data-memory access stages, and a register file write-back stage.

An array processor described by NEC in the "Static memory for high-bandwidth systems" session shows great performance potential thanks to high degrees of on-chip parallelism coupled with high integration levels. The same can be said for a neural-network processor presented by Mitsubishi in the "Neural networks and image sensors" session, as well as a neural-network processor from Tohoku University, Sendai, Japan, described in detail in the "Technology directions: memory, packaging" session.

NEC's biCMOS array processor delivers a peak execution level of 3.84 gigainstructions/s. It contains 64 simple processor elements and 2 Mbits of static RAM. Targeted at low-level image-processing applications, the array operates as a single-instruction, multiple-data (SIMD) parallel processor.

Each processing element (PE) consists of an 8-bit ALU, a shifter, some registers, a 4-kword-by-8-bit block of local memory, and a logic circuit for multiplication through the use of a lookup table. The register block includes a memory data register and an index register, both of which are used for memory accesses, two shift registers for serial-data transfers, several general-purpose registers for storing temporary data, a mask register to hold masking bits during a comparison operation, and an inter-PE register that aids in transferring data across adjacent PEs.

To simultaneously transfer data to all PEs from the local memory or send results to the memory, 512 sense amplifiers would typically be needed. However, 512 sense amplifiers simultaneously activated would cause a considerable current spike and consume lots of power. To minimize the power, designers at NEC came up with two strategies. First they access only half of each word at one memory-access instruction, and second, the word is accessed twice as fast as the PE clock.

With that combination, designers can reduce the number of sense amplifiers by 75%. But the amplifiers that are used must be fabricated with bipolar devices to achieve the high speeds needed—data transfers take place at 1.28 Gbytes/s when the SRAMs are clocked at 80 MHz. The chip's peak power can then be kept to about 4 W. The average power is actually much lower (about 1.8 W) because the memory blocks and their associated support circuits can be put into a low-power standby mode when not needed.

Twelve parallel FPUs delivering an aggregate throughput of 1.2 GFLOPS form the heart of Mitsubishi's neural-network processor. The dozen 24-bit FPUs tie in with a nonlinear function unit and a control block on the chip. The overall architecture allows the circuits to accelerate the convergence of calculation, reducing the number of typical neural operations by up to 69%. Neural tasks requiring over one million synapses can be executed using multiple copies of the chip together with additional memory chips.

As with NEC's array processor, this neural chip is also an SIMD processor. Each FPU packs its own local memory of 1.28 kwords by 24 bits. The PEs communicate with their neighbors through a shift-register ring. Such a scheme is promising for neural-network accelerators because both feed-forward and error back-propagation processes can be executed efficiently.

The chip's control unit includes a three-stage pipelined sequencer, a 1-kword-by-24-bit instruction memory, and a 256-word-by-144-bit microcode

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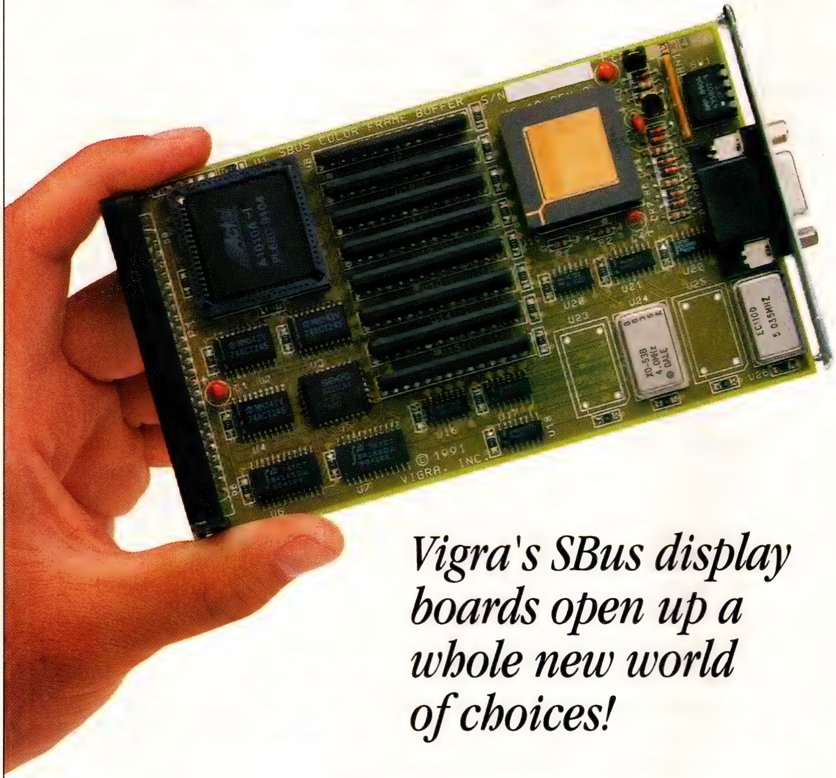

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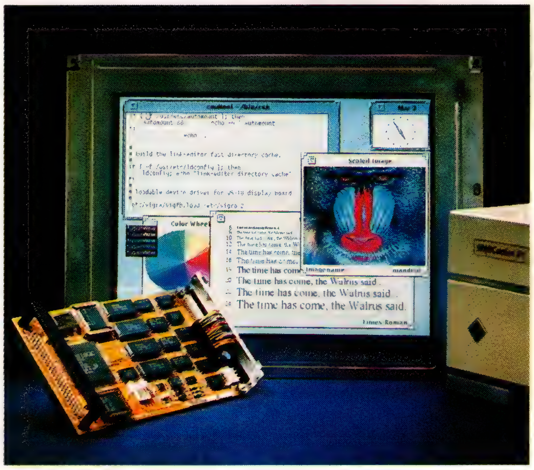
The time has come, the Walrus said.
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VS15 COLOR FRAME BUFFER with VGA Feature Connector Digital Output lets you use 640 x 480, flat electroluminescent or gas plasma displays with your SparcStation™. The Device Driver has color to gray scale conversion.

VS11 COLOR FRAME BUFFER with 76 Hz refresh rate capability matches high performance monitors from 640 x 480 to 1280 x 1024.

VS10 COLOR FRAME BUFFER has programmable resolution 640 x 480 to 1152 x 900 to match VGA, S-VGA, and Multisync displays. Display 256 colors from a palette of 16.7 million.

Vigra

Division of VisiCom Laboratories, Inc., 6044A Cornerstone Court, San Diego, CA 92121 • (619) 597-7080 *Fax: 619-597-7094* memory. That unit broadcasts the network parameters (learning coefficients or temperature parameters) or addresses for local memories through both a data and an address bus. Two external memory ports and a ring-expansion port permit networks of almost any size.

Tohoku University banks on a new memory technology that's been briefly described at conferences over the last year or so. The university's researchers crafted a multiple-valued memory technology that acts like brain neurons to perform intelligent fully parallel data processing. The memory technology quantizes analog input data and stores the data as multiple-valued representations.

Moreover, data association and classification according to the degree of association can also be performed at the memory-cell level without any software manipulation. Making such an intelligent data-processing cell possible is the novel Neuron MOS transistor, a multifunctional device implemented in a standard double-polysilicon CMOS process that can simulate the action of biological neurons.

A simple two-transistor cell used in a Neuron-MOS multivalued dynamic RAM consists of a gain-cell structure that delivers a high signal-to-noise ratio when reading—a particularly critical issue in multivalued circuitry *(Fig. 5a)*. Data on the bit line (the voltage level) is written to the cell by turning the write transistor (MW) on so that the floating-gate potential on the read transistor (MR) is the same level as the voltage on the bit line. Consequently, the data is "stored" on the floating gate of transistor MR *(Fig. 5b)*. That transistor has its threshold voltage set equal to the supply voltage.

To read data from the cell, the word line is set to the supply voltage, raising the floating-gate potential to the bit-line voltage plus the supply voltage thanks to capacitive coupling. That situates transistor MR into a source-follower configuration, which places a voltage back onto the bit line. That bit line newly placed voltage is identical to the original voltage stored on the floating gate.

Furthermore, the read is non-destructive—the charge stored on the gate remains. As a result, the problem of maintaining a sufficiently high storage-to-bit-line capacitance ratio in conventional DRAMs doesn't apply. If fabricated with the same 0.25-μm design rules as used for 256-Mbit DRAMs, the Neuron MOS gain cell requires less than one-third the area of the one-transistor cell used for standard DRAMs. The smaller area could ultimately pave the way for gigabit-generation memories.☐

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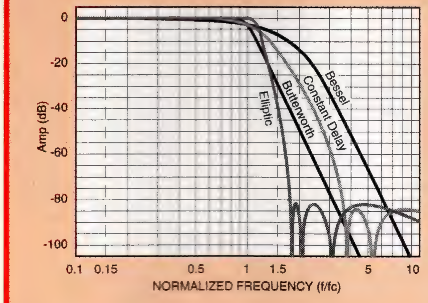

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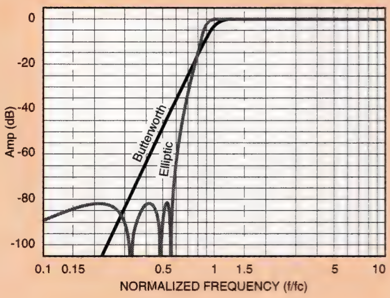

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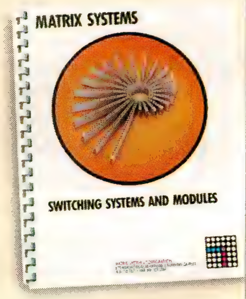

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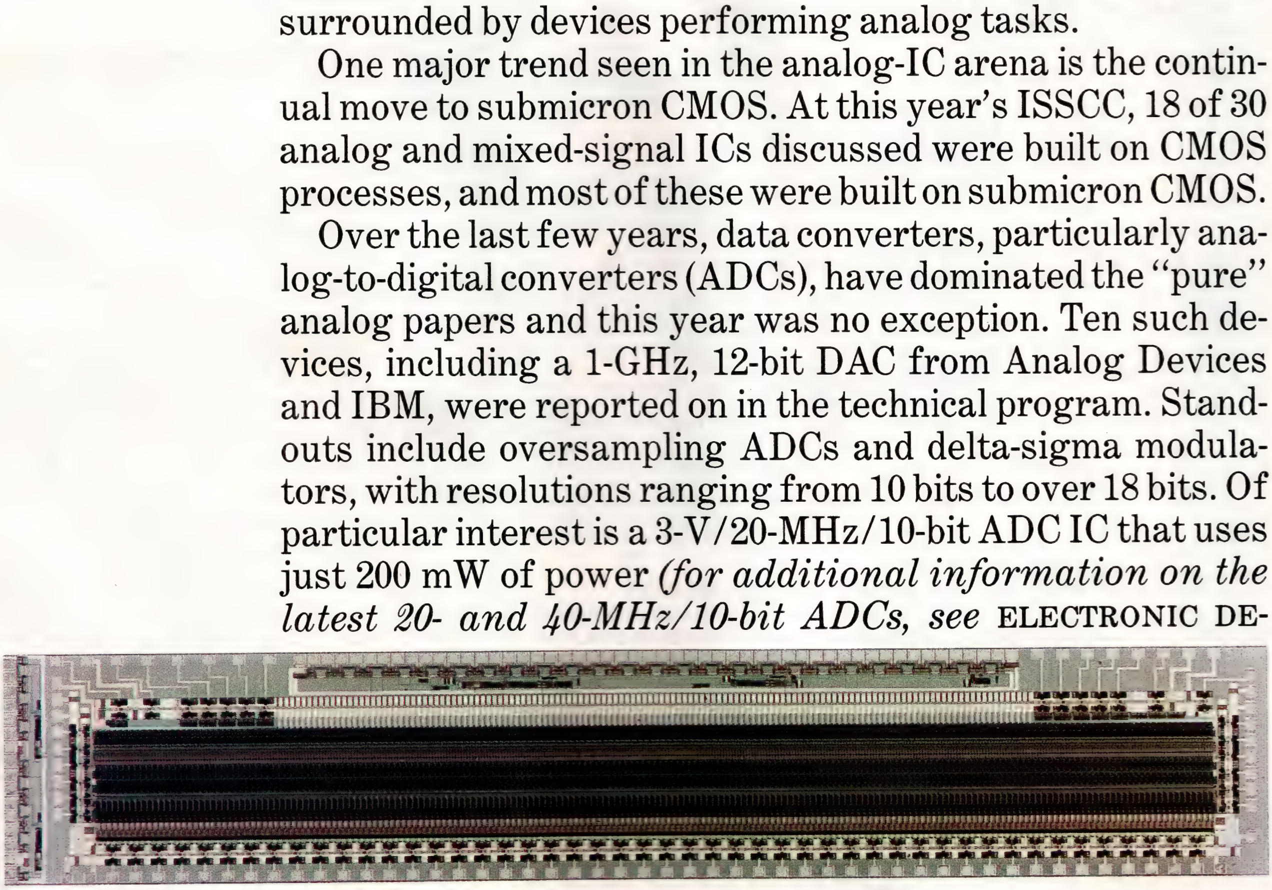
ISSCC

ANALOG TECHNOLOGY

As always, the analog papers at the annual ISSCC offer a cavalcade of riches for analog system designers. This year, they reached a new peak with representation in all three of the invited papers of the plenary session. Needless to say, *the real world is analog.* As truly complete systems on a chip become more prevalent, digital circuits, though they dominate a chip's silicon area, increasingly find themselves surrounded by devices performing analog tasks.

One major trend seen in the analog-IC arena is the continual move to submicron CMOS. At this year's ISSCC, 18 of 30 analog and mixed-signal ICs discussed were built on CMOS processes, and most of these were built on submicron CMOS.

Over the last few years, data converters, particularly analog-to-digital converters (ADCs), have dominated the "pure" analog papers and this year was no exception. Ten such devices, including a 1-GHz, 12-bit DAC from Analog Devices and IBM, were reported on in the technical program. Standouts include oversampling ADCs and delta-sigma modulators, with resolutions ranging from 10 bits to over 18 bits. Of particular interest is a 3-V/20-MHz/10-bit ADC IC that uses just 200 mW of power *(for additional information on the latest 20- and 40-MHz/10-bit ADCs, see* ELECTRONIC DE-



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SIGN, *Jan. 24, p. 123)*. In addition to the 1-GHz, 12-bit DAC, two others were detailed: a 1-GHz, 10-bit bipolar device, and a triple 8-bit unit in CMOS that updates at 320 MHz.

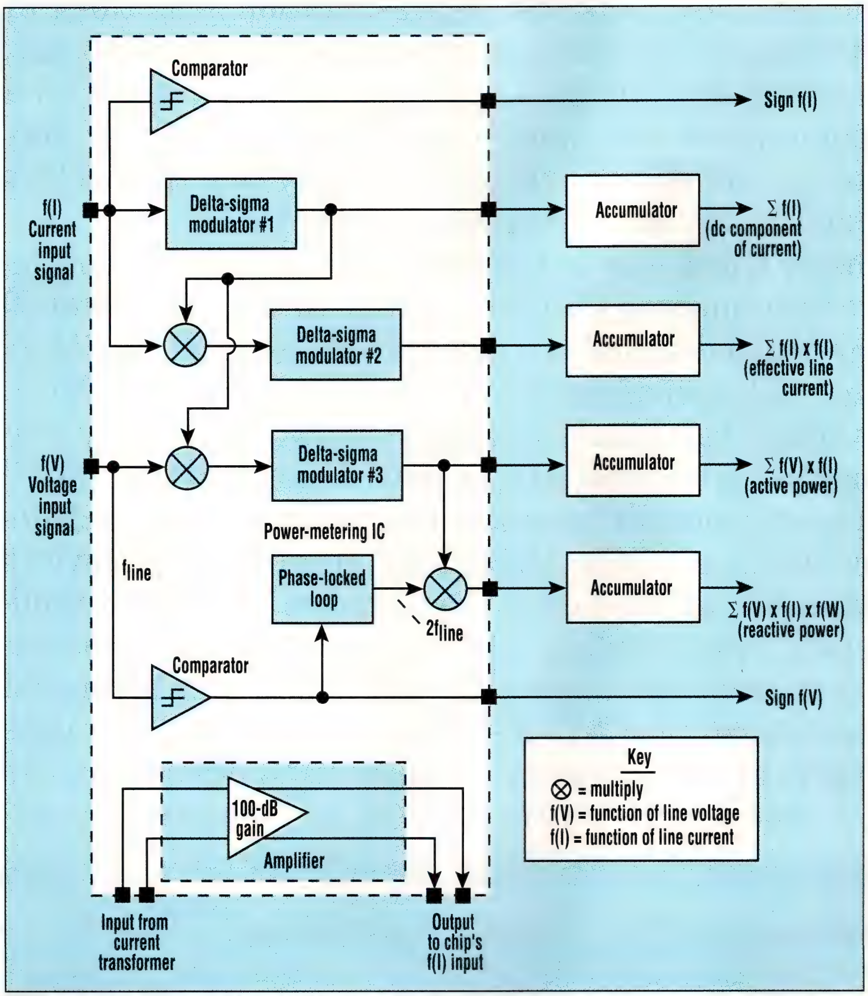
FAST AMPLIFIERS

Various amplifiers found their way onto the ISSCC's agenda, including the venerable sample-and-hold amplifier (SHA), which is considered by many to be the most difficult analog circuit to design. One intriguing SHA was designed for a pure analog application in thin-film-transistor liquid-crystal displays (TFT LCDs). This single IC contains 192 SHAs sampling at 60 MHz with a 40-MHz bandwidth. The 192 channels match within 3.5 mV rms.

Other amplifier discussions range from a pair of micropower CMOS op amps operating from as low as 1.1 V, to a 500-MHz-bandwidth GaAs-MESFET transimpedance amplifier, to several preamplifiers for magnetic storage. Although those two micropower op amps consume less than 300 μA of quiescent current, they're true op amps with open-loop gains beyond 80 dB and unity-gain bandwidths beyond 6 MHz. One of them puts out 3 mA.

An entire session is devoted to six hard-disk-drive (HDD) read-channel ICs. Continuing a major industry trend, five of these, used for data/clock recovery, employ partial-response maximum-likelihood (PRML) pulse detection. The sixth is a 3-V preamp with a 110-MHz bandwidth.

A mixed bag of other advances round out the analog portion of the ISSCC. For instance, an accurate, stable, and integrated RC time reference for use in continuous-time filters, oscillators, and multivibrators is discussed. Also unveiled is a 500-MHz time digitizer with a resolution of 15.625 ps; switched-capacitor and switched-current filters, both of which sample at 80 MHz; and a 2-V/200-mW bandgap reference built on a 0.65-μm CMOS process. Moreover, a handful of circuits built on a 1.2-V/0.3-μm CMOS process are covered. These range from a double feed-forward phase-compensated amplifier and an SRAM sense amplifier to a 9-bit/2-MHz/4-mW ADC.


Comparator
Sign f(I)
f(I) Current input signal
Delta-sigma modulator #1
Accumulator
Σ f(I) (dc component of current)
Delta-sigma modulator #2
Accumulator
Σ f(I) x f(I) (effective line current)
f(V) Voltage input signal
Delta-sigma modulator #3
Accumulator
Σ f(V) x f(I) (active power)
Power-metering IC
f_line
Phase-locked loop
2f_line
Accumulator
Σ f(V) x f(I) x f(W) (reactive power)
Comparator
Sign f(V)
100-dB gain
Amplifier
Key
⊗ = multiply
f(V) = function of line voltage
f(I) = function of line current
Input from current transformer
Output to chip's f(I) input

1. MULTIPLYING MODULATORS measure ac line power to within 0.1% accuracy. The output of 2nd-order delta-sigma modulator #3 represents a function of power, made up by the product of current input f(I) and the voltage input f(V).

OVERSAMPLING ADCs

Oversampling ADCs and delta-sigma modulators continue to improve to satisfy a wide assortment of new applications. Development highlights include:

- Resolution that has diverged from 16 or 18 bits to range from 10 to more than 20 bits.
- An input-signal bandwidth that has diverged from between a few hertz and 20 kHz to over 80 kHz. In fact, one device provides a 192-kHz bandwidth. Another, a 10-bit narrowband delta-sigmal converter, possesses a 30-kHz bandwidth centered at 1.8 MHz.
- Applications that diverge from classic high-resolution dc instrumentation systems, seismic systems, and consumer audio to electrical-power metering, professional audio, high-frequency data acquisition, and high-resolution medical imaging.
- Delta-sigma converters that are becoming available from a number of suppliers.

Designers of oversampling ADCs are using many different architectures to improve ADC performance. For example, in one session, four CMOS and three biCMOS ADC ICs are described. Three of these use 4th-order modulators (two of which consist of cascaded 2nd-order pairs). A fourth one, a 6th-order modulator, employs a trio of cascaded 2nd-order pairs and tri-level quantization. A 5th-order current-sensing modulator starts with a 1st-order delta-sigma loop and follows it with two 2nd-order pairs. In addition, a 10-bit device uses a single 2nd-order loop, and a power-metering chip contains multiplying 2nd-order delta-sigma loops.

Some of the ICs contain only the

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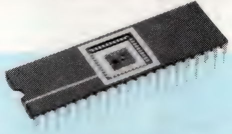

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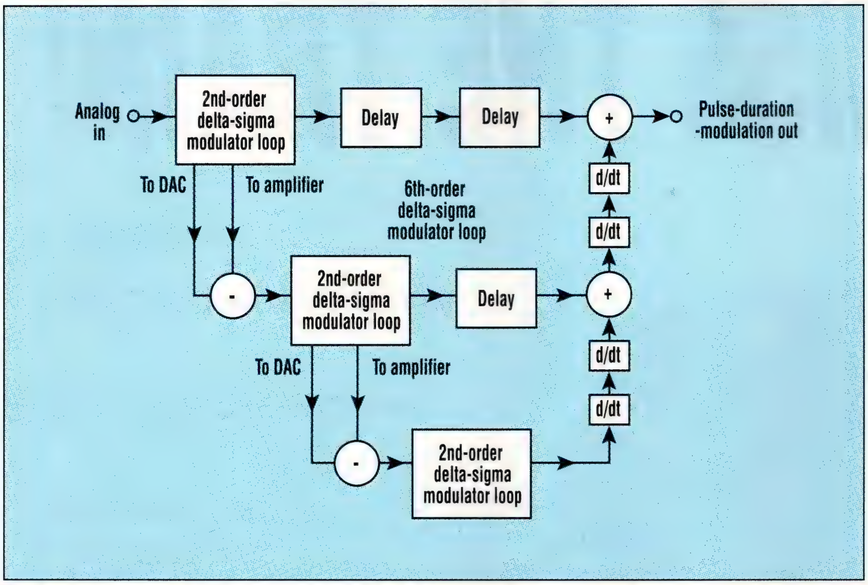

Analog in
2nd-order delta-sigma modulator loop
Delay
Delay
+
Pulse-duration -modulation out
To DAC
To amplifier
6th-order delta-sigma modulator loop
d/dt
d/dt
-
2nd-order delta-sigma modulator loop
Delay
+
To DAC
To amplifier
d/dt
d/dt
-
2nd-order delta-sigma modulator loop

2. THREE 2ND-ORDER DELTA-SIGMA MODULATOR loops are combined to create a 6th-order delta-sigma modulator with a 100-kHz signal bandwidth.

delta-sigma modulators and rely on external digital-signal processors or microprocessors for integration and/or digital filtering/decimation. Some complete converters consist of chip sets with an analog modulator chip and a digital filter chip. And, some converters integrate both the modulator and filter on one chip.

METERING THE AC LINE

Electric utilities are becoming more interested in replacing the conventional electro-mechanical watt-hour meter with an electronic circuit for remote meter reading. To increase the efficiency of power distribution, the metering circuit must not only be able to measure active power, but also simultaneously measure reactive power, the dc component of the line current, the effective line current, the power factor, and all line-signal harmonics up to the 40th.

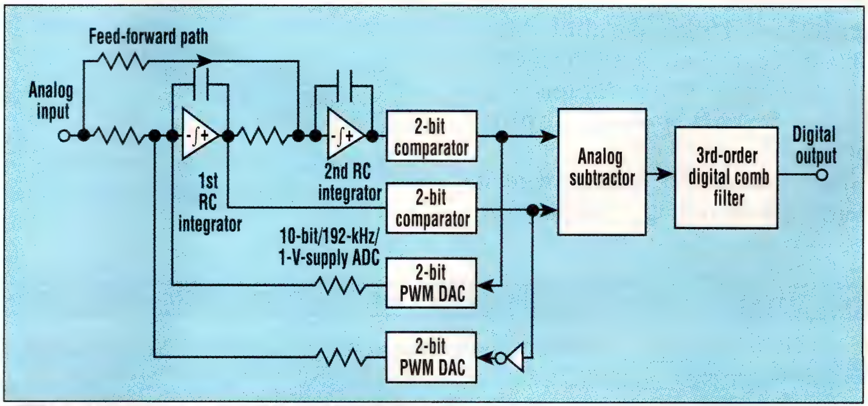
In the classical approach, the momentary line current and voltage are applied to a pair of delta-sigma ADCs, and their product is calculated in the digital domain. Digital accumulators perform the integration. To obtain accuracy to within 0.1% over a 300:1 current range and a 3:1 voltage range, 20-bit delta sigma converters with 10-bit accuracy must be employed.

For the electronic-metering circuit, an IC designer at Mietec Alcatel, Brussels, Belgium, came up with an alternate approach. He developed a multiplying 2nd-order delta-sigma modulator that converts the product of two analog signals (voltage and current, for example) directly into a digital format representing power *(Fig. 1)*. Transformers connected to the line provide the voltage and current signals. Working together, the chip's three modulators perform two multiplications. The 1-bit output of modulator #1 determines the dc component of the line current. Modulators #1 and #2 form a multiplying circuit that produces a function of the effective line current at the output of modulator #2.

Similarly, modulators #1 and #3 provide a function of the active power consumption at the output of modulator #3. Adding a pair of zero-crossing comparators determines the sign of the voltage and current inputs. The output of the line-frequency-doubling, digital phase-locked loop (PLL) multiplied by modulator #3's output provides a signal representing a function of the reactive power. The chip also contains a high-gain differential amplifier for use between a current transformer (or a current-sensing resistor) and the chip's current input. The digital circuitry (accumulators) is implemented off chip.

The IC is built on a biCMOS process and runs off ±5-V rails. The sampling clock operates at 200 kHz. Averaged over 100 seconds, the integral linearity of the multiplying ADC runs 30 ppm of full scale, with the line voltage and current at 80% of full scale. Under similar conditions, phase error is less than 0.00002° and reactive-power full-scale error is less than 5% of full scale.

In contrast, to achieve wide bandwidth and high resolution while minimizing the oversampling ratio, a designer at Fujitsu's European Design Center, Maidenhead, Berkshire, England, cascaded three 2nd-order delta-sigma modulators, thus creating the analog (modulator) section for a 6th-order delta-sigma ADC *(Fig. 2)*. It combines a 90-dB signal-to-noise ratio (SNR) with 100 kHz of bandwidth. The high oversampling ratios (often as great as 64) typically required for 16-bit or greater delta-sigma ADCs usually lead to power-



3. ADDING A FEED-FORWARD PATH and employing continuous-time integrators permits this 10-bit oversampling ADC to run off a 1-V battery. The converter has a 192-kHz signal bandwidth and handles 400-mV p-p signals.

hungry op amps and digital filters, as well as hard-to-drive signal and reference inputs. On the other hand, a lower oversampling ratio (OSR) can result in linearity and stability problems due to component mismatch. Or, when handling large signals, it can lead to quantizer overload. The Fujitsu device, which provides 6th-order noise shaping while operating with an OSR of just 16, needs just 40 mW of power.

To approach the theoretical dynamic range possible from cascaded delta-sigma loops, the first loop should use a 2nd-order circuit. This would provide enough noise shaping to avoid precision component matching. Each successive loop reduces the noise by performing a conversion on the quantizing errors created in the previous loop. Each of the three 2nd-order loops in the Fujitsu IC employs a three-level (two-comparator) quantizer. These offer improved SNR over a single-level (1-bit) circuit without the need for ultra-linear DACs required by higher-level quantizers. To combine loop outputs, each loop adds a one-sample analog delay and doubly-differentiates quantization noise. Using a single amplifier for both integrators in each 2nd-order loop reduces the amplifier's required slew rate, as well as the IC's power and silicon area. This can be done by switching integrator capacitors (a cute circuit trick only possible with switched capacitors). The chip is built on a 1.2-µm biCMOS process.

A team from National Semiconductor, Santa Clara, Calif., created a 16-bit delta-sigma ADC on one chip complete with digital filters and a bandgap reference. The converter, which sports an input signal bandwidth of 84 kHz, is aimed at precision sampling of signals well beyond the audio range. These include professional audio equipment, communications test equipment, and high-speed data acquisition.

The IC cascades a pair of 2nd-order delta-sigma modulators whose outputs are combined to create a 4th-order modulator operating with an OSR of 64. A two-stage digital filter decimates the composite output. The combiner cancels the 2nd-order-shaped quantization noise of the first modulator and reshapes the second modulator's quantization noise to the 4th order, leaving the signal component unchanged. Like the previous device, the architecture isn't sensitive to mismatch errors between the components (MOS capacitors) forming the first-stage integrators. The converter is built on a 5-V, 1-µm biCMOS process whose npn transistors have f_ts of 6.5 GHz.

1-V-RAIL OVERSAMPLER

To achieve the lowest-possible power drain and run off 1-V batteries, two designers at NTT's LSI Laboratories, Kanagawa, Japan, employed a 1-V, 0.5-µm CMOS process to build oversampling 10-bit ADCs and DACs. The converters can be used in digital cordless telephones and low-cost portable digital audio systems. Capable of building 10-MHz CMOS logic, the process offers both conventional and low-threshold-voltage MOSFETs. The trick was to create analog circuits that could run off a 1-V rail without losing accuracy due to reduced dynamic range and bandwidth, and poor switching in the switched-capacitor circuits.

To do the job, NTT's designers modified a conventional delta-sigma architecture by adding a new feed-forward path, creating what they call "swing-suppression" noise shaping *(Fig. 3)*. Besides the new feed-forward path, the circuit uses op amps to replace the switched-capacitor integrators in the 2nd-order modulator with continuous-time RC integrators. The feed-forward path creates true 2nd-order noise shaping and suppresses the phase shift in the first integrator. The feed-forward path also nulls out any of the analog input signal appearing at the second-integrator input. This, in turn, suppresses the second integrator's output swing by 35%, reducing the integrators' susceptibility to overload.

While running off a supply rail between 0.8 and 2 V and sampling at 6.14 MHz, the ADC combines 10-bit resolution with a 192-kHz signal bandwidth. It has an OSR of 16, a dynamic range of 58 dB, and can handle analog input swings of 0.4 V p-p. Power consumption with the digital filter runs a minuscule 1.8 mW. An oversampling DAC with similar performance needs under 1 mW.

A different problem—accurately sensing and digitizing a wide range of currents—faced two designers at Crystal Semiconductor, Austin, Texas. Such currents, like those from photodiode sensors employed in medical imaging, can range from 1 pA to 1 µA, a 120-dB (1 million to 1) dynamic range. To accurately sense and digitize this six-decade range of current, thermal-noise currents at the system inputs must be minimized. Typical systems employ a classic transimpedance amplifier (a FET-input op amp connected as an I-to-V converter) followed by a high-resolution ADC. In an optimized system, the thermal-noise current is dominated by the feedback resistor. The lower the current to be measured, the larger the feedback resistor and the greater the error due to current noise.

Crystal's designers developed a 5th-order delta-sigma modulator that encloses a transimpedance amplifier within its output-to-input loop *(Fig. 4a)*. The switched-capacitor C-DAC functions as a "feedback resistor." The effective thermal noise is equal or less than that of the largest feedback resistor, which can be used while operating from ±5 V.

Theoretically, the current noise from a switched-capacitor resistor is the same as that of the real resistor it emulates (within the same bandwidth). However, this analysis assumes that the capacitor is charged and discharged every clock cycle. The tri-level quantizer in the C-DAC's modulator lowers the effective current noise about 1.5 dB. It operates the middle quantizer in a "do nothing" state that dumps the C-DAC to ground, thus not delivering thermal-noise charge to the input summing point *(Fig. 4b)*. The coefficients represented by a_1 through a_5, and b_1 and b_2, perform noise shaping.

However, the tri-level quantizer gives up the inherent linearity of the more conventional two-level (1-bit) quantizer. If not corrected, intermodulation of quantization noise near one-half the sampling frequency (126 kHz) will be aliased back into the band of interest (dc to 492 Hz). Even nonlinearities of 0.05% can render the tri-level quantizer unusable.

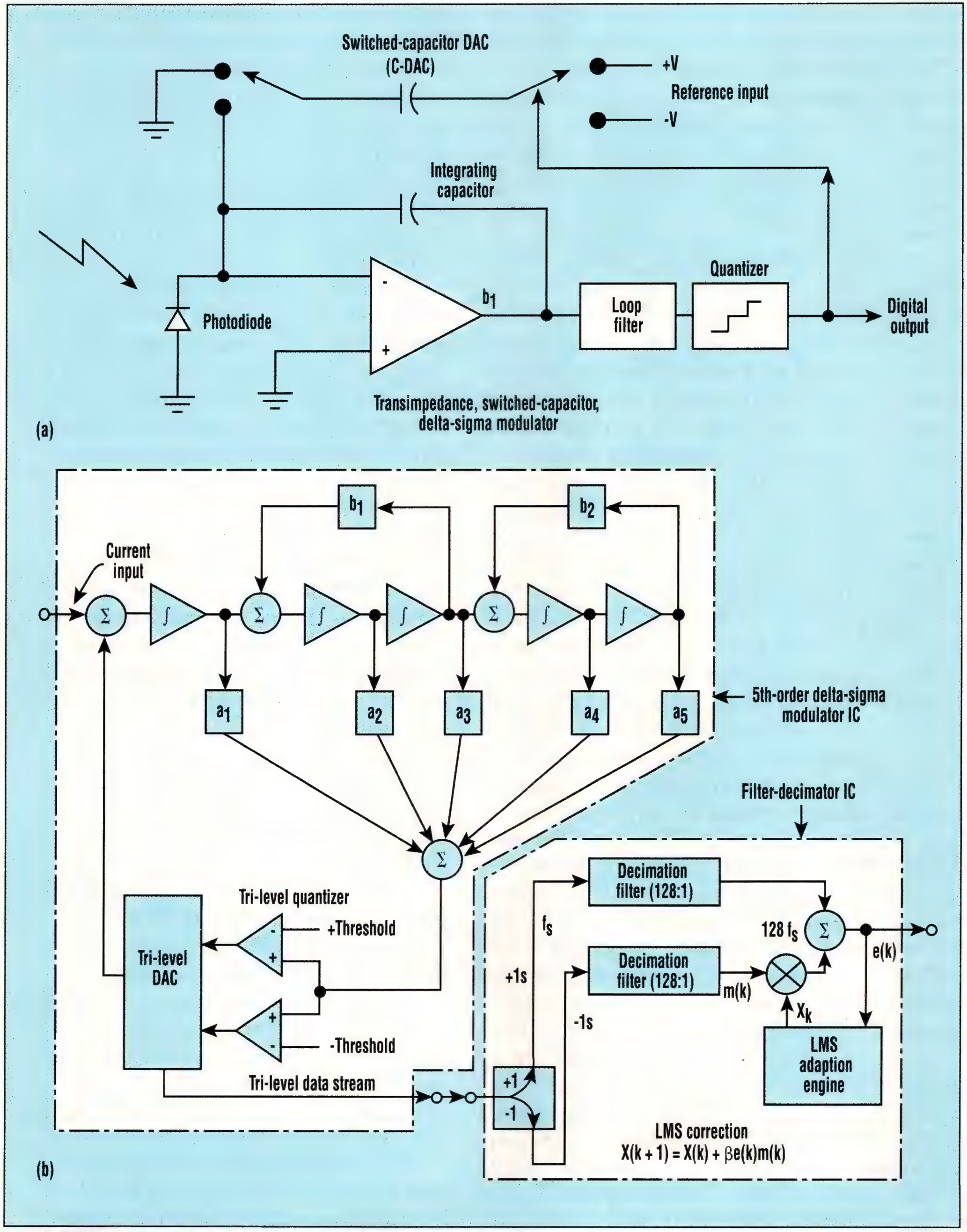
The correction is performed in the

companion filter-decimator (digital) chip. First, the tri-level data stream from the 5th-order delta-sigma modulator splits into two paths. Then positive Ones are routed to one decimation filter and negative Ones to a second decimation filter. Zeros are applied to both filters. Multiplying the negative Ones by the correction factor X_k corrects the data. During a calibration cycle, the least-mean-squares (LMS) adaption engine using an LMS algorithm converges on a value for X_k and stores it in a register. Normal operation follows this sequence. Each output sample from the negative-Ones filter is summed with those from the positive-Ones filter, yielding a 20-bit output.

In the 492-Hz passband, the input-current noise floor runs 76 fA/$\sqrt{\text{Hz}}$ while full-scale current is 1.38 μA RMS, a dynamic range of 118 dB. Although shown as single circuits on each chip, the modulator is actually a dual circuit and the filter chip handles the output of eight modulators. Thus, an eight-channel chip set contains five chips, four dual modulators, and the octal digital-filter chip. The modulator die is built on a 2-μm CMOS process while the filter die is built on a 0.8-μm CMOS process.

Low-frequency measurement applications demanding low power consumption, wide dynamic range, and high linearity tend to migrate to oversampling ADCs. One such task is sensing and digitizing seismic activity, which needs a signal-to-distortion ratio of at least 120 dB. A second team of designers from Crystal designed a switched-capacitor, delta-sigma modulator with a single-ended linearity of better than 120 dB. The integrated quantization noise in the 400-Hz band runs –125 dB relative to full scale using an OSR of 128. Chopper-stabilizing the first integrator eliminates 1/f noise.

The modulator's designers chose a relatively conventional 4th-order design using a 1-bit quantizer. Meeting the distortion requirements meant that a number of refinements had to be made at the circuit level to attack known distortion mechanisms (generally not significant in most other applications) in switched-capacitor topologies. Because seismic systems don't require dc response, the modulator adds double polysilicon input-coupling capacitors. Their nonlinear voltage coefficient is minimized with a back-to-back structure. In such a structure, two equal capacitors are connected in parallel, but the polarities are reversed.



4. A LOW-NOISE TRANSIMPEDANCE delta-sigma modulator is built by replacing the amplifier's feedback resistor with a switched-capacitor DAC (a). The technique can create a 5th-order modulator that senses currents from 80 fA to 1.40 μA (b).

ANALOG SAMPLING

Sampling (and holding) doesn't necessarily imply quantization. Like Nyquist's and Shannon's concepts, SHAs arrived long before ADCs and digital computers. In fact, vacuum-tube ver-

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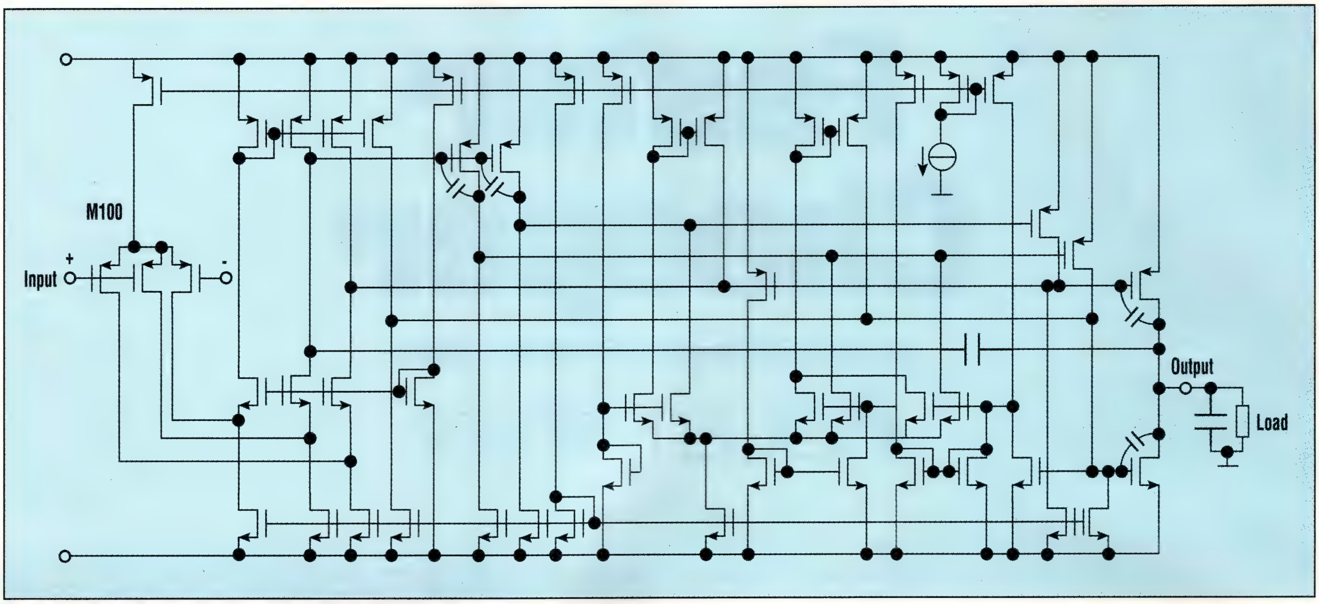
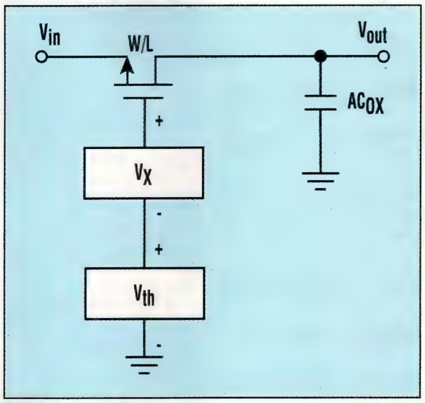


5. THIS FOUR-STAGE CMOS OP AMP operates from 1.1-V supply rails. It draws 15 μA and slews at 0.7 V/μs.

sions called "boxcar integrators" handled radar and nuclear instrumentation during and after World War II. Now "massively parallel" SHAs are finding their way into LCD color-TV and computer screens. Each pixel gets its input from the analog voltages stored in a trio of SHAs, one each for the red, green, and blue (RGB) colors. A design team at Toshiba's R&D center, Kawasaki, Japan, put 192 of these SHAs on a single CMOS IC built on a 0.8-μm process *(see the opening figure)*. This long and skinny chip is less than 0.1-in. wide and over 0.5-in. long (2.47 by 13.5 mm, or 97.2 by 531 mils).

Each SHA drives the 100-pF wiring capacitance to its load, an amorphous-silicon TFT on the LCD, which in turn drives the pixel capacitance. Pedestal errors caused by differences in offset between SHAs on the same chip, or between chips, severely distort the colored picture. They're caused by differences in the MOSFET's channel charge and gate-signal feedthrough. To eliminate these errors, each SHA incorporates a charge-compensation circuit using 15 MOSFET switches driven by a 5-phase clock. In actuality, two SHAs are operated in parallel. While one samples its input, the other drives an output-buffer amplifier.

The output buffer for each SHA pair is disconnected from the sampling circuit and its 100-pF load until the signal is sampled and the charge error compensated. The buffers sport a 3-dB bandwidth of 60 MHz. While sampling at 95.5 MHz, the chip dissipates less than 100 mW when each SHA drives its 100-pF load. Channel matching runs better than 3.5 mV RMS.



6. THIS **temperature-stable integrated RC time constant uses the on-resistance of the MOSFET for the R value. An on-chip oxide capacitor is employed for the C value.**

Although the Toshiba chip handles LCD screens, color-CRT displays for computer graphics keep increasing in pixel density with the goal of ultimately achieving film-quality images. As a result, the video DACs driving them must keep climbing in speed. With that in mind, a designer at Analog Devices, Wilmington, Mass., created a triple 8-bit video DAC that updates at 320 MHz, making it suitable for 3-Mpixel displays. A 360-MHz version can handle 4 Mpixels. The DAC takes in 40-MHz data and upconverts it to the high clock rate. Built on a 0.8-μm CMOS process, it dissipates less than 2 W.

When operating at 320 MHz, the DAC's power dissipation must be kept under 2 W in order to use low-cost plastic packaging. As a result, the DAC employs multiple data paths at sub-pixel clock rates.

The technique offers other advantages. For example, dual paths running at 160 MHz were chosen for the main portion of the chip. Running the circuits at 320 MHz would severely limit the number of gates allowed between registers. But at 160 MHz, a reasonable quantity of gate delays can be inserted between registers, and the 320-MHz rate doesn't have to be sent over the whole chip.

In addition, a synchronous rather than a skewed design can be used, eliminating timing hazards from slow and fast circuit paths. The area penalty of dual data paths is less than expected because smaller cells can be used. The 8-bit digital words are ultimately fed to a pair of decoders. One decodes the four MSBs into the drive for 15 current sources, and the other performs a similar function for the four LSBs. The triple DAC also includes a PLL to increase the clock from 40 MHz to 320 MHz, an 8:1

input multiplexer, and the hardware to implement an X-Window-compatible 64-by-64-by-2 cursor function. Integral and differential nonlinearity (INL and DNL) for the chip run better than ±0.4 LSB.

Direct digital synthesis (DDS) of RF signals represents another application for video DACs. But DDS systems need 10 to 12 bits of resolution to minimize spurious harmonics, or "spurs." And some graphics tasks are asking for similar performance—all at ever higher update rates. To meet those needs, a design team from Philips Research Labs, Eindhoven, the Netherlands, created a 1-GHz, 10-bit DAC built on an 11-GHz bipolar process. The DAC dissipates 730 mW from a 4.5-V supply.

The chip's architecture represents a trade-off between minimum glitch impulse and minimum nonlinearity. Its five MSBs are segmented with row and column decoders. Bits 8 and 9 form the row decoder, and bits 5, 6, and 7 form the column decoder. The decoded lines drive 31 identical current sources. Using the row and column technique simplifies the circuit and minimizes large variations in delays among the outputs. The technique compensates for existing delays. The five LSBs drive similar current sources, which in turn drive a 50-Ω R2R network. INL and DNL run better than 0.35 LSB and all "spurs" run 58 dB below the fundamental. Glitch-impulse runs less than 1 pV-s—about the same as the energy in a 0.5-LSB output updated at 1 GHz.

Over the past decade, teams of designers from Delft University of Technology, Delft, the Netherlands, have developed unique and high-performance bipolar op amps that operate from ever lower supply rails. Now they've turned their attention to CMOS op amps. One paper describes a pair of op amps designed to run off a 3-V rail. A second paper presents a slower op amp designed for a 1.5-V rail. The latter device has also been characterized at 1.1 V.

The 3-V op amps draw 180 μA of quiescent current, can put out ±3 mA, and run off supply voltages between 2.5 and 6 V. Input common-mode voltage can run to within 500 mV of the plus and minus rails. The outputs can swing to within 200 mV of the plus rail and 100 mV of the minus rail. The op amps' open-loop gain is 86 dB. The pair differ mainly in their compensation, which affects unity-gain bandwidth and slew rate. One device employs Miller compensation while the faster one uses cascoded Miller compensation. Unity-gain bandwidth for both is 2.6 and 6.4 MHz, respectively, and slew rates are 2.3 and 4.1 V/μs. Both are built on a 0.8-μm CMOS process.

CMOS op amps have traditionally employed cascode circuits (like the aforementioned devices) to achieve maximum gain with a minimum number of gain stages. With this method, though, designers soon run out of head room when using supply voltages much below 2.5 V, and cascoding thus becomes impossible. As a result, the designers of the 1.5-V op amp turned to a unique 4-stage design with no more than one saturation voltage inside a gate-source voltage *(Fig. 5)*. Compensation is provided by the five capacitors shown in the circuit, a technique they call "multipath hybrid-nested Miller compensation." The "multipath" input stage is implemented via transistor M 100 and the folded-cascode circuit that follows it.

When operating with 1.5 V between the plus and minus rails and driving a 10-kΩ/10-pF load, the op amp features a quiescent current of 290 μA, maximum output current of 5 mA, an output-voltage swing that's within 200 mV of both rails, and an offset of 4 mV. Under the same conditions, the open-loop gain is 120 dB, unity-gain bandwidth is 6 MHz, and the slew rate is 13 V/μs. Dropping the supply voltage to 1.1 V while driving the same load yields a quiescent current of 15 μA, a maximum output current of 500 μA, an offset of 4 mV, open-loop gain of 120 dB, unity-gain bandwidth of 0.6 MHz, and a slew rate of 0.7 V/μs.

Precision IC filters, oscillators, and multivibrators need accurate and stable time constants, which in all but high-frequency applications are usually derived from off-chip RC, LC, or crystal-resonator time references. That's because the simplest and most common integrated time constant is the product of resistance and capacitance. Unfortunately, on-chip resistance and capacitance can vary from 30 to 50% with process and/or temperature changes. Moreover, many applications demand an order of magnitude less variation, and would benefit from the elimination of external parts and their package pins.

A designer from Philips Semiconductors, Sunnyvale, Calif., came up with a technique that builds these time constants on a biCMOS process. It uses mobility as a time standard to develop a resistance that's temperature-stable and inversely proportional to oxide capacitance. Mobility is slightly sensitive to doping concentration and very sensitive to temperature. It varies as the "minus-three-halves" power of the temperature. However, this can be compensated for with a number of well-known circuit techniques. For example, in a simple low-pass filter section, assuming that $V_{in} = V_{out} = 0$ at dc:

$$\begin{aligned} t &= C(R_{on}) \\ &= A(C_{OX})L/[\mu C_{OX} W(V_{gs} - V_{th})] \end{aligned}$$

where A is the capacitor area, V_{th} is the MOSFET's threshold voltage, μ is the dielectric constant, and L and W are the dimensions of the FET's gate *(Fig. 6)*.

Because $V_{gs} = V_{th} + V_X$, this simplifies to:

$$t = LA/\mu W V_X$$

The filter cutoff frequency will now be temperature stable if V_X is designed with a temperature drift inversely proportional to mobility. The task of designing a temperature-stable time reference now becomes one of designing a temperature-stable voltage reference—which is well known. Scaling can be performed with either the FET's W/L, its nominal value of V_X, or the capacitor area. So far, the technique has been used to build a one-shot multivibrator IC whose nominal 5.5-μs delay varies less than 0.3 μs between −40 and +40°C.☐

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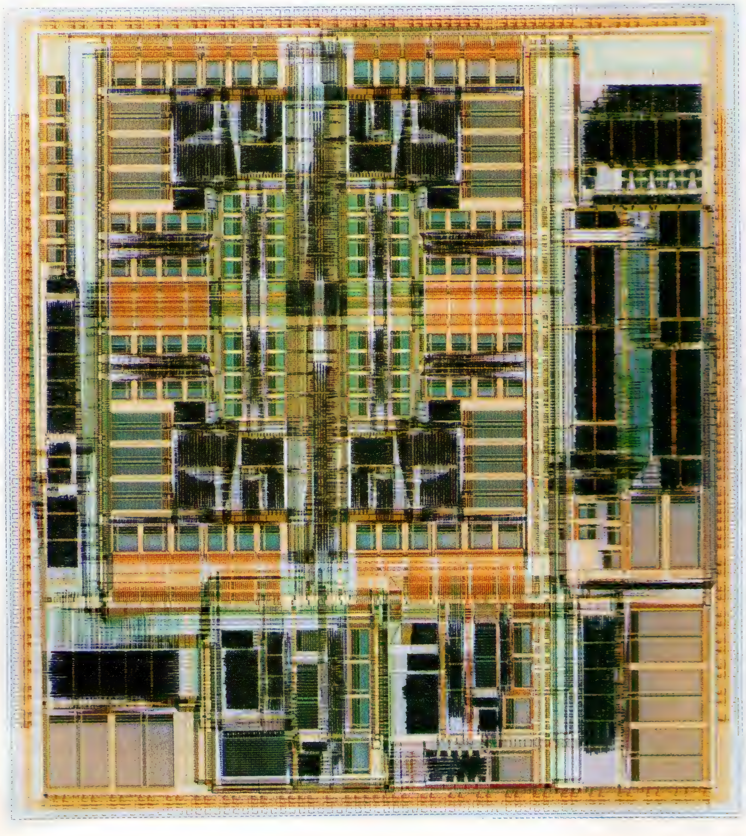
I S S C C

COMMUNICATIONS TECHNOLOGY

Judging from the papers at the three ISSCC communications sessions, the microelectronics industry seems more than ready for any challenges the National Information Infrastructure and its foreign counterparts can throw at it.

In the field of video codecs, MPEG-2, the second generation of the standard created by Motion Picture Experts Group, has pushed researchers to produce some very impressive digital-signal-processor chips. Single-chip implementations of the standard require advanced process technology, such as triple-level metal, 0.5-μm geometry, as well as processor power of 200 MIPS. Wireless communications and optical communications also will be part of the information infrastructure of the future, even though they stand at opposite ends of the communication hierarchy. Papers in the wireless session mostly address RF front ends with aggressive processing technologies that can handle gigahertz-level transmission while operating at lower supply voltages. Process technology also plays a big role in the fiber-optic communications session, in which III-IV



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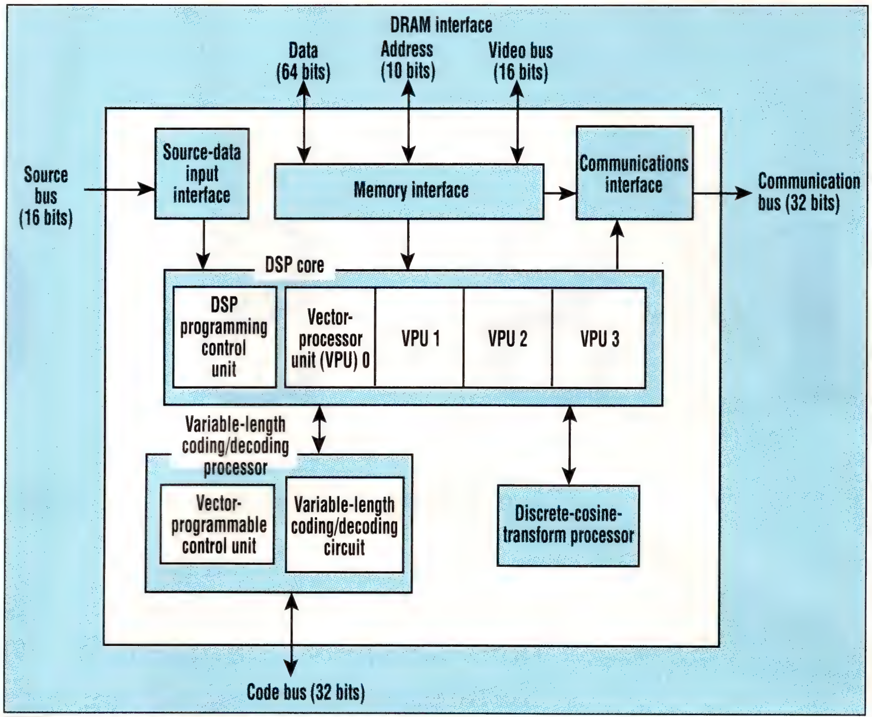
devices other than gallium arsenide are receiving attention.

As might be expected, chip architects have turned their attention to high-definition TV (HDTV) and the MPEG-2 video compression encoding/decoding scheme in a big way at this year's ISSCC. Interest in the second-generation coding scheme, promulgated by the Motion Picture Experts Group (MPEG) of the International Standards Organization, is high. That's because it can, in fact, handle HDTV data rates and its picture quality has apparently satisfied the television industry.

The chips offering these solutions boast higher levels of integration and impressive 200-MIPS performance, but perhaps the most interesting of the video chips at the ISSCC comes from the Integrated Circuits and Systems Lab of the University of California at Los Angeles. Even as MPEG grows in acceptance, questions persist not only about its ability to compete with schemes based on fractals and wavelets, but also on MPEG's ability to handle a wide range of applications. UCLA's Stephen Molloy and his colleagues addressed this problem, coming up with an 80k-transistor, configurable 25-Mpixel/s compression processor.

Architectural choices such as defining memory and I/O are the forte of the design, which specifically targets two-way communication of live video in a portable, wireless environment. Dedicated MPEG solutions that depend on higher levels of integration and more transistors are at a loss in the wireless context because they lack flexibility. The other common option—programmable video processors—are too complex for portable devices.


DRAM interface
Data (64 bits)
Address (10 bits)
Video bus (16 bits)
Source bus (16 bits)
Source-data input interface
Memory interface
Communications interface
Communication bus (32 bits)
DSP core
DSP programming control unit
Vector-processor unit (VPU) 0
VPU 1
VPU 2
VPU 3
Variable-length coding/decoding processor
Vector-programmable control unit
Variable-length coding/decoding circuit
Discrete-cosine-transform processor
Code bus (32 bits)

1. THE MPEG-2 PROCESSOR developed by Matsushita consists of a DSP core, variable-length coding/decoding processor, and a discrete-cosine-transform processor. The core includes a programmable control unit and four vector-processing units. The variable-length coding/decoding processor contains one programmable control unit and a dedicated circuit to execute variable-length coding and decoding.

Flexibility is important in the wireless environment because different algorithms exhibit superior performance in specific applications. One-way retrieval of stored video, for example, lends itself to vector quantization (VQ), because the low complexity of VQ provides dramatically lower power consumption. For two-way video communication, on the other hand, subband coding offers better image quality at low bit rates than the basic 8-by-8-pixel block used by the discrete-cosine-transform (DCT) algorithm for MPEG because subband coding doesn't exhibit blocking artifacts. MPEG is still in the picture, however, because it will be needed for compatibility with traditional video sources.

The proposed video-compression-processor unit (VCPU) from UCLA follows a strategy of configuring signal flow by determining the control overhead, on-chip memory sizes, and I/O bandwidth needed to provide a given throughput. For example, the coefficient and pixel/data memories are configured as dual-ported line memories. Each provides eight operands to the sum-of-products unit on every clock cycle. This architectural choice markedly reduces memory complexity in both the address bandwidth and the number or required ports.

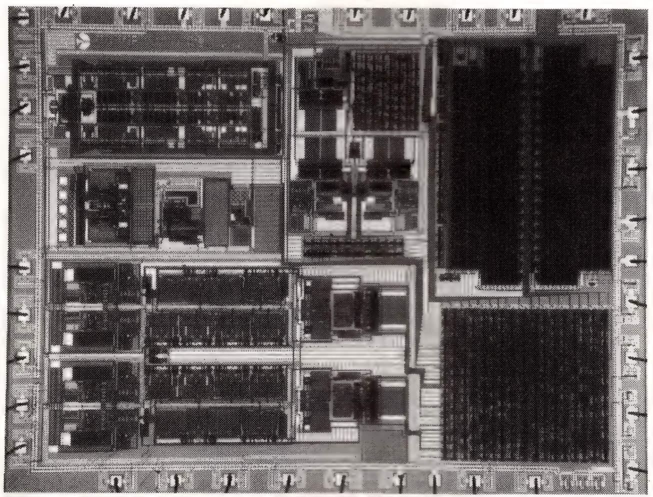
Its flexibility is quite impressive. The authors provided figures of merit for executing various decompression algorithms. Its relative efficiencies are 40%, 70%, and 95% of existing dedicated ASICs for executing DCT, 8-by-8 FIR filtering, and vector quantization, respectively.

Although the design can be pushed to 25 Mpixels/s, it's more likely to run at 5 Mpixels/s in a wireless application. It has been tested to a maximum clock rate of 50 MHz, and uses robust circuit techniques as well as 1.2-μm CMOS technology.

Two dedicated MPEG-2 chips—the first silicon to implement the standard—will debut at the ISSCC. A single-chip solution created by Toshiba Corp., Kawasaki, Japan, applies relatively exotic technology to the problem with the expected high-performance results. The decoder is fabricated in 0.5-μm triple-level metal and packs 1.1 million transistors into a 225 mm^2 die. When driven at 70 MHz, it can decode HDTV video despite its wider aspect ratio. The chip is designed, however, to handle decoding at the CCIR 601 rate of 720-by-480 pixels/frame. It requires 4 Mbits of external DRAM, which is used as a rate buffer, for reference pictures and display buffers.

Engineers at Matsushita Electric Company Ltd.'s Semiconductor Research Center, Osaka, Japan, used the same fabrication process (0.5

μm, triple metal) for their chip and also borrowed an architecture from the parallel-processing world. Their video digital signal processor for MPEG-2, called the VDSP2, uses a programmable DSP core and a two-level parallel-processing architecture. The chip combines a macroblock-level pipeline with a single-instruction, multiple-data (SIMD) type vector-pipeline architecture. Each macroblock consists of the basic unit of MPEG-2 chrominance and luminance in a 16-pel-by-16-pel domain. By using the SIMD scheme, the programmable DSP core can process a macroblock within the real-time time constraints.



2. THIS ANALOG FRONT END for the IS-54 cellular standard used in the United States is fabricated in 1-μm double-poly CMOS. Created by Rockwell, it uses a single 5-V supply and includes an on-chip differential bandgap reference and a 2.5-V reference generator. Power dissipation is 100 mW.

The processor is made up of three distinct processing units: the DSP core; a variable-length coding/decoding processor; and a DCT processor *(Fig. 1)*. The DSP core includes one programmable control unit and four vector-processing units. The variable-length coding/decoding processor has one programmable control unit and a dedicated circuit to execute variable-length coding and decoding. In addition to the standard DCT circuit, the processor contains a clipping circuit and sequencer.

The chip runs at 100 MHz and possesses 200 MIPS of processing power. A single chip can be employed to implement a decoder; two running in parallel can be used for an MPEG-2 decoder. The chip's 3.3-V power supply keeps the power consumed by its 2.5-million transistors down to 4.2 W at 80 MHz.

While the developments from Toshiba and Matsushita depend primarily on process technology to achieve their goals, a design from M. Matsui and his colleagues at Toshiba's Semiconductor Device Engineering Laboratory, Kawasaki, Japan, takes a novel approach. The chip addresses the DCT algorithm and can be used to decompress MPEG-2, HDTV, or JPEG. Running at 200 MHz on a 3.3-V supply, the DCT unit alone consumes 0.35 W. When operating at 100 MHz on a 2-V supply, it consumes 0.15 W.

The low power consumption and small area are achieved by implementing a sense-amplifying pipeline flip-flop (SA-F/F) circuit instead of normal CMOS circuits. The differential input voltage of the SA-F/F is just 100 mV. Consequently, the threshold voltage drop by NMOS pass-transistors doesn't hinder the function of the circuit even in low-voltage operation. The gains achieved are impressive: a 20-bit adder, for example, has about a 30% area advantage over CMOS circuits and a 50% speed advantage. M. Matsui is presently a visiting professor at Stanford University, Palo Alto, Calif., and can be contacted at the university's STAR laboratory.

Other papers in the session include an analog CMOS teletext data slicer from Philips Research labs, Eindhoven, The Netherlands, and a 100-MHz, 5-Mbaud quadrature-amplitude-modulation (QAM) decision-feedback equalizer for digital TV applications. The QAM chip developed by UCLA is intended for products such as HDTV and the proposed high-definition cable TV that require data rates of up to 30 Mbits/s. In order for digital TV to be compatible with the existing 6-MHz NTSC channel bandwidths, compression is required. In addition, the channel impairments of cable and broadcast TV means both transmission modes suffer significant intersymbol interference and require adaptive equalizers. The QAM adaptive equalizer from UCLA can handle 4-, 16-, 64-, and 256-QAM formats. At a top clock rate of 100 MHz, the equalizer maximum symbol rate is 5 Mbaud.

It's evident from the collection of ISSCC communications papers that wireless modalities are pushing the leading edge for both design and fabrication technology. No fewer than five papers were presented on RF analog front ends that operate at up to 2 GHz. The other papers were spread equally between IF chips for cellular communications and spread-spectrum applications.

CHIPS FOR WIRELESS

Among the analog front ends, one of the most interesting is a direct-conversion modulator that runs at 2 GHz off a 2-V supply. The chip, which was designed at Nippon Telegraph and Telephone (NTT) Ltd.'s LSI Laboratory in Kanagawa, Japan, effectively breaks the 5-V barrier for Si-bipolar direct-conversion quadrature-modulator circuits. Past problems have involved the Gilbert-cell-based, double-balanced mixers used in 5-V solutions because they require a high supply voltage. When the supply voltage of a Gilbert-cell mixer is reduced, it severely affects linearity and modulation accuracy.

NTT's new circuit is what the inventors call a "current-folded" double-balanced mixer, or CF-DBM. The modulator consists of a core and a 90° phase shifter. The modular core, in turn, integrates two CF-DBMs, a summing circuit, and a differential output buffer. The CF-DBMs are differentially driven by signal-to-balance converters (SBCs), which receive local signals from the phase shifter that are 90° out of phase. The modulator boasts a wide bandwidth of 0.8 to 2 GHz and consumes 68 mW.

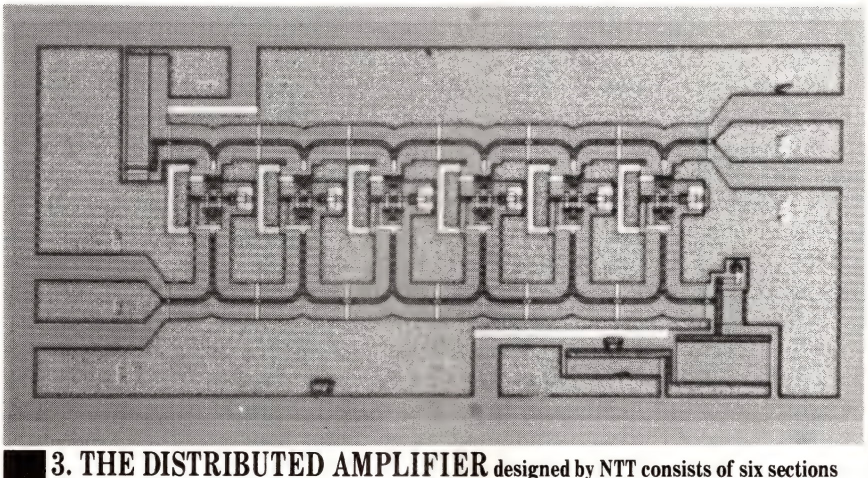
In its most simple explanation, low-voltage operation is achieved by reducing the number of series-connected transistors in the CF-DBM. Although the CF-DBM has some similarities to a Gilbert Cell, it uses only two series-connected transistors. The CF-DBM draws about 15% more current than a Gilbert Cell. The modulator employs a self-aligned Si-bipolar process with a cutoff frequency of 18 GHz. As a result of the lower voltage supply, the chip consumes about one-third the power of 5-V solutions, but more important, the 2-V supply makes battery operation easier to design in.

Another paper that breaks new ground in analog front ends comes from Matsushita Electronic Corp.'s Research Laboratory in Osaka, Japan. This one, however, describes how gallium arsenide can be used in a monolithic RF switch without the distortion experienced in previous solutions when transmission power increased. Historically, conventional Si PIN-diode switches tend to consume undesirable power because the current bias must increase as transmitting power rises. On the other hand, GaAs switches have been demonstrated that operate with very low power dissipation, but the waveform is subject to distortion as transmission power increases.

A new circuit configuration developed at Matsushita allows the GaAs switch to handle more than 5 W with an insertion loss of less than 1.0 dB. Previous GaAs switches have endured power problems because of the FETs' threshold voltage. In particular, a negatively biased control voltage must be overcome for switching to occur. The RF single-pole, dual-throw circuit solves this problem by superimposing a synchronized voltage to the control gate. This is accomplished by connecting a feed-forward capacitor and a diode in series between the control gate, the FET, and the signal input. Positive voltage switching is performed by integrating large coupling capacitors at the input and output terminals.

Process technology also is important in Matsushita's chip, which allows four large bypass capacitors, each 100 pF, to be squeezed into a relatively small area. The result is a very small, 10-pin package with lead spacing of 0.5 mm—the smallest reported for this application.

Three other papers in the wireless communications session addressed designs for analog front ends. Designers from Alcatel Bell Telephone, Antwerp, Belgium, describe a two-chip set, one CMOS and the other bipolar, that integrate all of the basic front-end functions for a 1.9-GHz mobile telephone. The bipolar chip integrates a quadrature generator, receive-and-transmit mixers and amplifiers, and a 64/65 prescaler. It has a die size of 8 mm^2. The CMOS chip, 40 mm^2, executes all of the low-frequency baseband signal processing and frequency synthesis. Total power dissipation of the chip set is 250 mW in receive mode and 400 mW in transmit mode. To obtain a fast settling time for the synthesizer, Alcatel engineers invented a new circuit that includes a current-output, digital-to-analog converter.



3. THE DISTRIBUTED AMPLIFIER designed by NTT consists of six sections of unit cells, each having a cascode circuit of FETs to achieve high output impedance. This reduces the drain-line attenuation and provides higher amplifier output gain. A frequency-dependent termination is implemented at the end of the output drain line to provide a more even gain over the device's frequency range of dc to 10 GHz. A variation of 2 dB using conventional terminations was reduced to just 0.5 dB.

A transmitter chip for digital cellular applications designed by Hewlett-Packard Co., Newark, Calif., and Ericsson GE Mobile Communications Inc., Research Triangle Park, N.C., substantially reduces the number of process technologies needed to implement a digital cellular transmitter for handsets. Typically, CMOS is used for baseband processing, GaAs for the power amplifier, and silicon bipolar for oscillators, amplifiers, frequency converters, and modulators.

The ISOSAT silicon bipolar technology used in the HP/Ericsson chip features transistors that can run as fast as 30 GHz in RF applications. As a result, the chip offers the highest level of integration to date for a transmitter RF IC. One feature of note is that the chip includes an almost completely monolithic PLL and VCO for the 70-to-200 MHz range (the exception is an external passive loop filter). The chip could be used in handsets destined for the North American 824-to-849 MHz digital cellular standard as well as the European Groupe Speciale Mobile (GSM) system of 890-to-915 MHz, and the 940-to-956 MHz Japan Digital Cellular (JDC). The HP/Ericsson chip uses a 5-V supply.

In a paper from Siemens AG Semiconductor Group, Munich Germany, the company describes a monolithic 2-GHz superheterodyne receiver that operates at 3 V and targets digital telephone applications or wireless LANs rather than cellular. The low operating voltage makes it more compatible with battery operation, yet the chip has been fabricated in a 7.5-GHz silicon bipolar process. The single superheterodyne solution was considered the best compromise between the options of double-frequency conversion and zero IF. Among the advantages cited by the speakers are low power consumption thanks to the fact that it has no second-stage synthesizer or mixer, fewer discrete components, and no crosstalk between the digital and IF stages.

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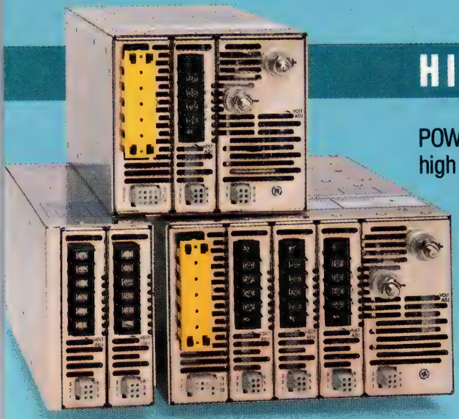

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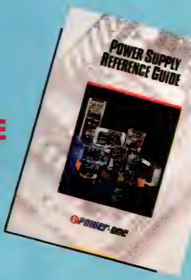

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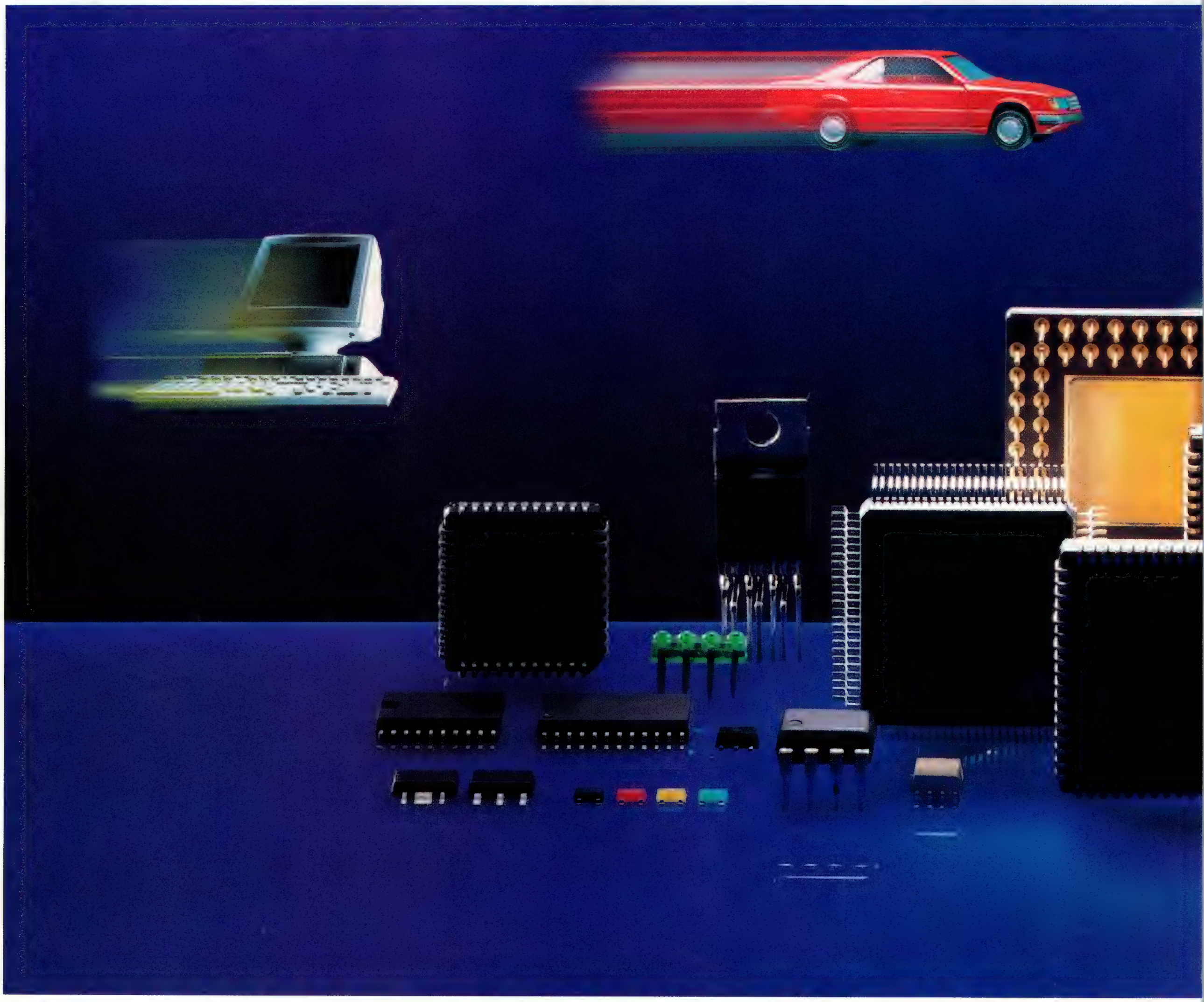

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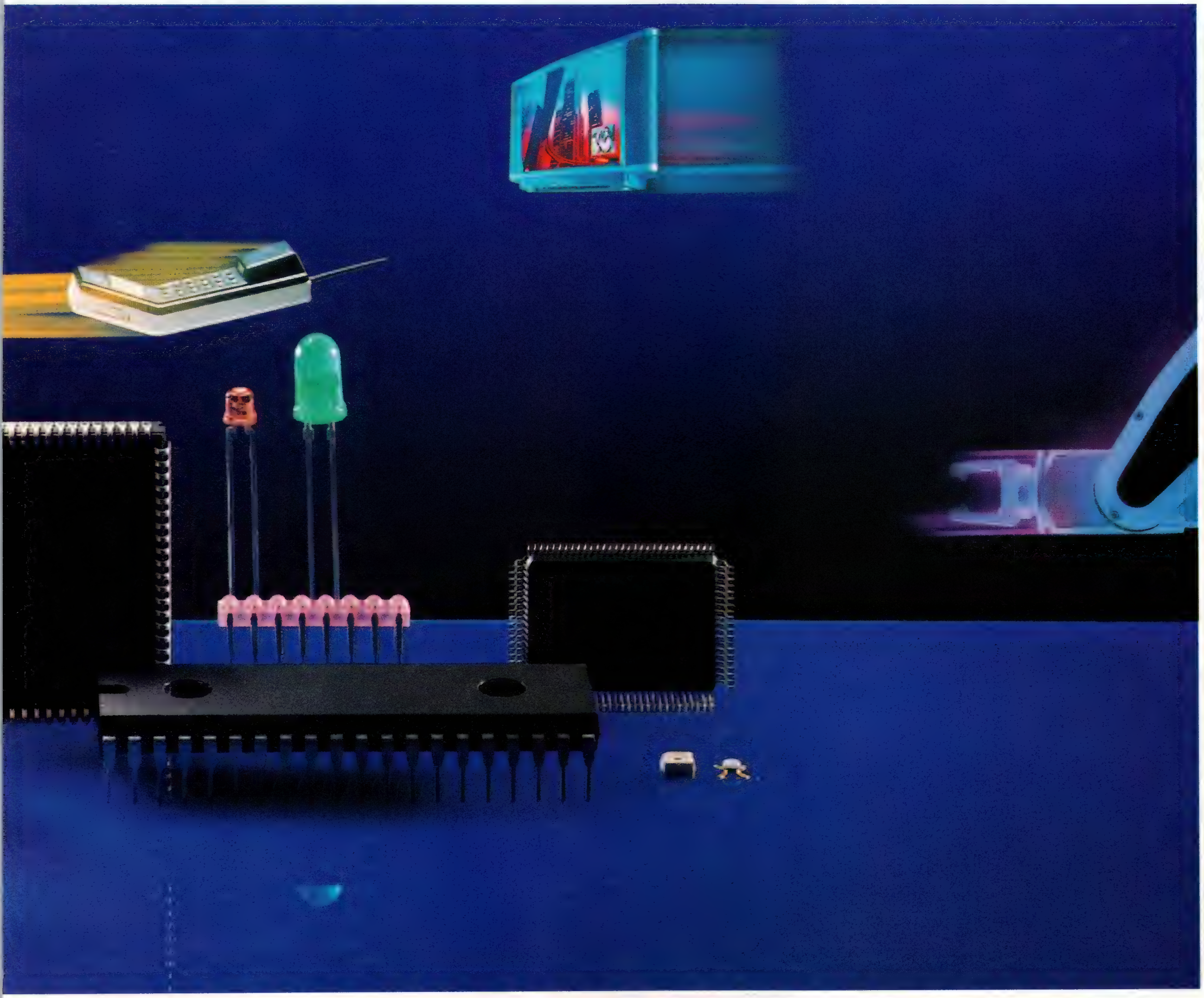

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digital cellular, analog cellular-phone technology is still attracting plenty of attention. A paper from Rockwell International Corp., Newport Beach, Calif., for example, describes a mixed-signal CMOS chip that demodulates in the RF digital domain using a delta-sigma architecture *(Fig. 2)*.

The importance of this chip, which addresses the North American IS-54 analog cellular standard, is that it neatly skirts the issue of using precision analog circuits. In conventional solutions, dual analog quadrature mixers are required to convert the receive signal from the second IF to baseband in order to maintain the requisite dynamic range. A simple bandpass filter provides antialiasing for the delta-sigma modulator, which has an IF of 1.8 MHz; a sampling frequency of 7.2 MHz; and a channel bandwidth of 30 kHz. The designers added 12 dB of programmable gain to the modulator's front end to increase the dynamic range of the receiver to 96 dB. The high dynamic range reduces the amount of programmable gain and, consequently, power dissipation and cost.

OPTICAL COMMUNICATION

The much-talked-about National Information Infrastructure (NII) for the United States is a high-profile example of the trend toward data bandwidths that can only be accommodated by fiber-optic media. For now, though, getting the information on and off the high-speed optical highway will still be the job of microelectronics. The ISSCC's optical communications papers, which conveniently divided themselves by process technology, discuss a 13.4-GHz frequency divider, a 622-Mbit/s termination chip for the Synchronous Digital Hierarchy (SDH), and a 240-Mbit/s optical receiver. One paper describes two chips—a 20-GHz decision IC and a 19-GHz preamplifier fabricated in silicon-bipolar technology. Three III-IV devices are presented: a GaAs MESFET, an indium-phosphide amplifier, and an indium-aluminum-arsenide/indium-gallium-arsenide high-electron-mobility-transistor (HEMT) amplifier with a bandwidth of dc to 60 GHz.

The InAlAs/InGaAs amplifier circuit developed by Nippon Telegraph and Telephone's (NTT) LSI Laboratories in Kanagawa, Japan, delivers the widest bandwidth of any device known *(Fig. 3)*. The chip demonstrates that certain problems associated with wide-bandwidth optical devices can be overcome by implementing a distributed architecture. For instance, when extremely wide bandwidths are encountered in optical systems, the wavelength of the electrical signal approaches the physical size of the package cavity, I/O leads, and bonding wires. The three-dimensional effects of these physical elements can be solved with a distributed configuration of the amplifier and a new package that reduces resonance. Similarly, the parasitic-capacitance problems created by using lumped constants in circuit design can be avoided by using a distributed-circuit architecture. As an amplifier, however, the chip leaves something to be desired inasmuch as its gain is 9 dB.

On the other hand, a paper coauthored by researchers in Hewlett-Packard Laboratories, Palo Alto, Calif., and Hughes Research Laboratories, Malibu, Calif., reports an amplifier with a high gain-bandwidth product that doesn't used a distributed architecture. It delivers 17 dB gain from 100 MHz to 70 GHz. The Hughes InP MMIC (Monolithic Microwave Integrated Circuit) process was implemented to fabricate the chip. The amplifier is a fully-integrated, three-stage, shunt-feedback design that achieves its performance largely due to the high transconductance and bandwidth characteristics of the InP process. However, InP's relatively poor gain is a problem. Researchers attacked the problem with a cascaded design using shunt-feedback cells for input and output and a common source interstage.

The third III-IV paper reports a 20-GHz, 8-bit multiplexer fabricated in a 0.5-μm GaAs process. Authored by researchers from Toshiba Corp.'s Research Labs in Kawasaki, Japan, it has a cutoff frequency of 40 GHz.

A CMOS chip from AT&T Bell Laboratories, Holmdel, N.J., is interesting in that it takes CMOS to new speed levels. The chip is a simple one-half frequency divider that runs at 13.4 GHz and is fabricated in a partially-scaled 0.1-μm process. Speed is attained by avoiding the types of structures that slows CMOS down. NMOS FETs are used for sensing and regeneration, and PMOS FETS for pull-up. The chip also avoids the capacitive-inducing techniques, such as the stacking of devices, and employs a ring-shaped geometry for all transistors to minimize capacitance. Running on a 2.8-V supply, it dissipates 28 mW at 13.4 GHz.

CMOS will establish itself as a contender in the commercial Sonet (Synchronous optical network) marketplace thanks to a chip from NEC Communication Systems Ltd., Chiba, Japan. This low-power multiplexer and demultiplexer operates at 622 Mbits/s and replaces four or five biCMOS or GaAs chips now used to terminate Sonet lines. The researchers developed a new multiplexer/demultiplexer architecture to both handle the speed and control power dissipation. A fast module handles the 622-Mbit/s serial data and converts it to 78-Mbit/s, 8-bit parallel data. In addition, by using this architecture, the number of transistors operating at 622 Mbits/s were reduced. CMOS-type gates were employed in modules that transmitted 311 Mbits/s or less, while NMOS gates handled 622-Mbit/s operations. Total power consumption of the chip is 5.7 W. It's fabricated in 0.8-μm CMOS and packaged in a 224-pin ceramic QFP.

Another CMOS chip, created by researchers at the Katholieke University of Leuven, Heverlee, Belgium, implements a 240-Mbit/s optical receiver. Because the photodiodes used to convert light to electrical signals typically produce currents in microamperes, a high transimpedance is needed to reject noise from digital circuits on the same IC. The chip offers a transimpedance of 150 kΩ at a bit rate of 240 Mbit/s for currents as low as 1 μA. If the input current is as high as 15 μA, the circuit can handle 490 Mbits/s with a transimpedance bandwidth product of 18 THzΩ.

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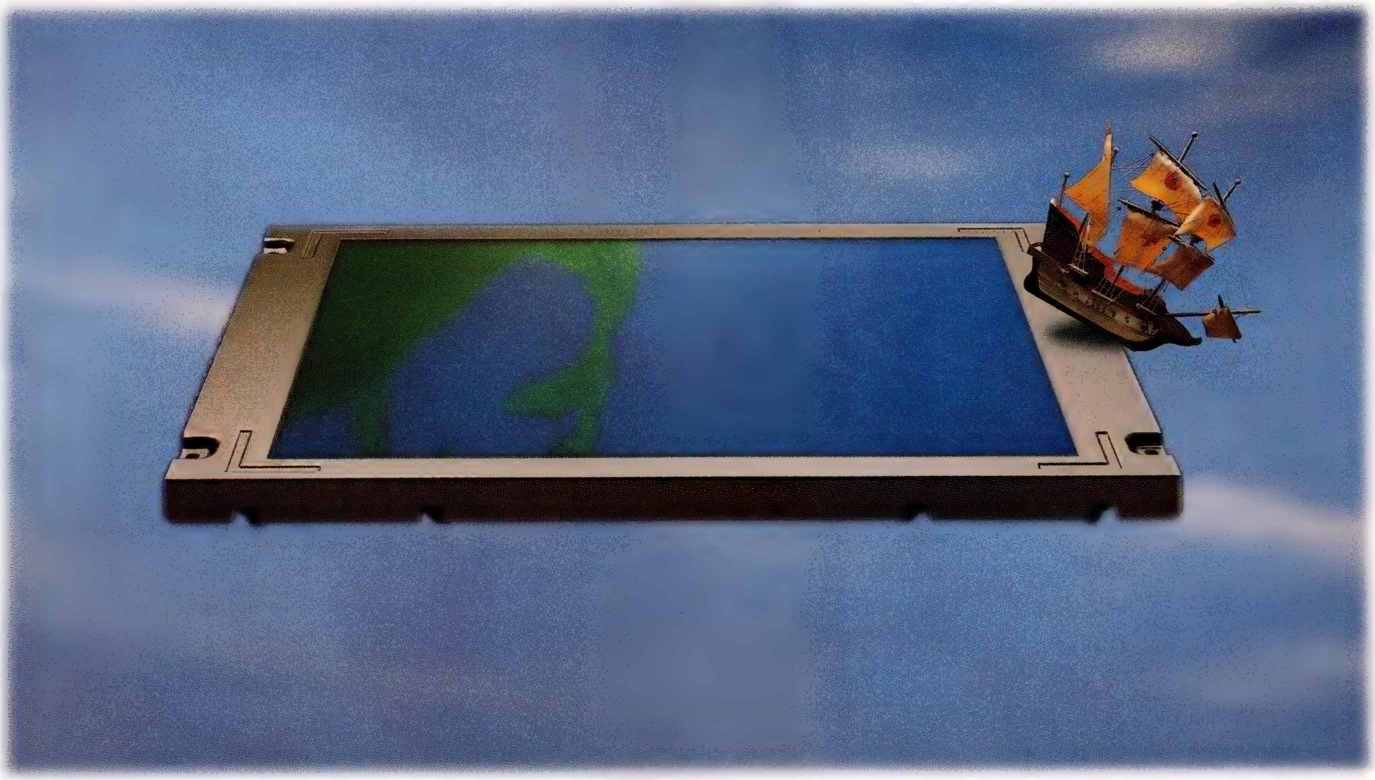

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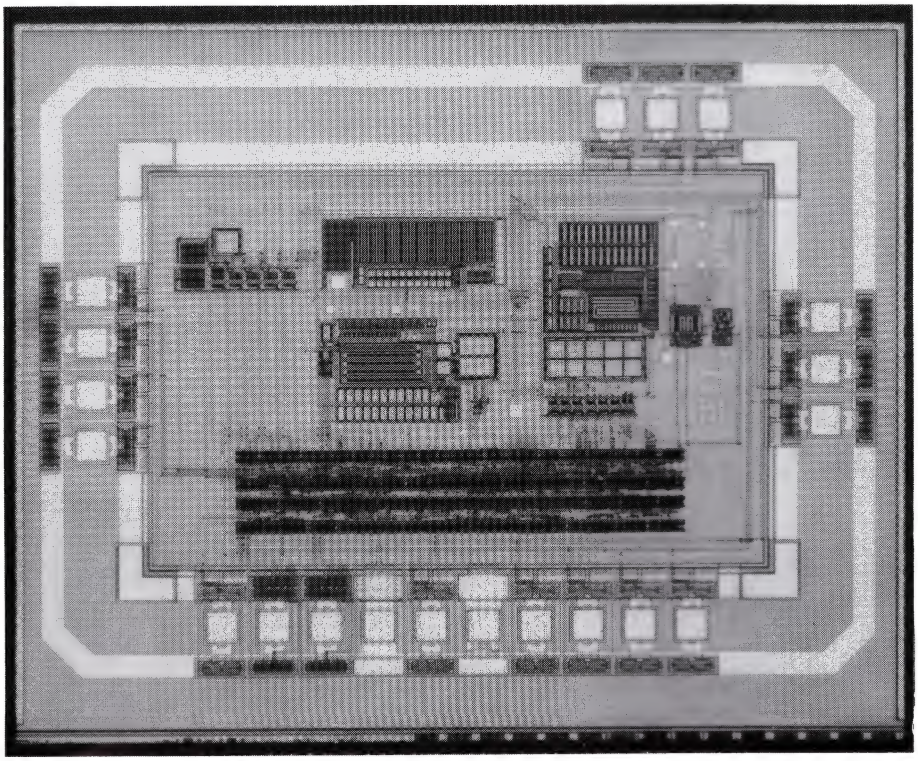
I S S C C

SENSOR TECHNOLOGY

Sensors, imagers, and displays usually are characterized by their wide variety of mixed-signal systems-on-a-chip. At this year's ISSCC, that tenet certainly holds true to form. What's interesting is that analog technology plays a significant role in virtually all of them, as many contain on-chip analog-to-digital converters (ADCs), modulators, or precision amplifiers. Moreover, with the exception of several focal-plane imagers, all are made with CMOS or biCMOS processes.

Representative sensor ICs include a 1-MHz, full-scale, light-to-frequency sensor that handles a 7-decade range of light intensity, and a ±1-g bulk-micromachined accelerometer in which the proof mass forms the heart of a 15-bit delta-sigma ADC. Other sensors consist of a closed-loop chemical-analysis device with an on-chip, 13-bit ADC that measures and controls the potential from an electrochemical cell, and a 32-channel charge-to-digital chip providing 17 bits of dynamic range.

The display arena of-



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PQFP	16 SOIC	20 SOIC	28 PLCC	44 PLCC	68 PLCC	84 PLCC	100 PQFP
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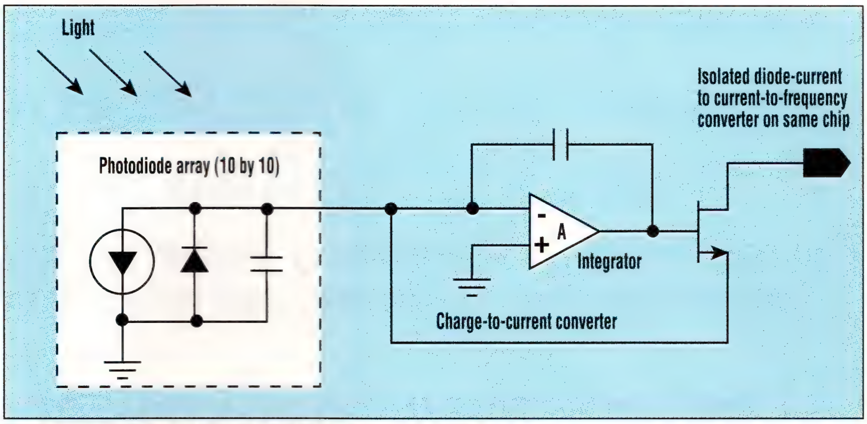

Light
Isolated diode-current to current-to-frequency converter on same chip
Photodiode array (10 by 10)
A
Integrator
Charge-to-current converter

1. A CHARGE-TO-CURRENT CONVERTER isolates the photodiodes from the readout circuit (a four-decade current-to-frequency converter) for a 10-by-10-diode light-intensity-sensing array, developed by Texas Instruments.

Imagers range from a trio of 2-million-pixel CCD-based imagers for portable HDTV cameras to a 64-by-64 (4096) pixel array of phototransistors, each driving its own first-order delta-sigma modulator. A functionally similar 32-by-32 (1024) pixel array replaces the phototransistors and modulators with photodiodes and light-to-frequency converters.

CHARGING CHARGES

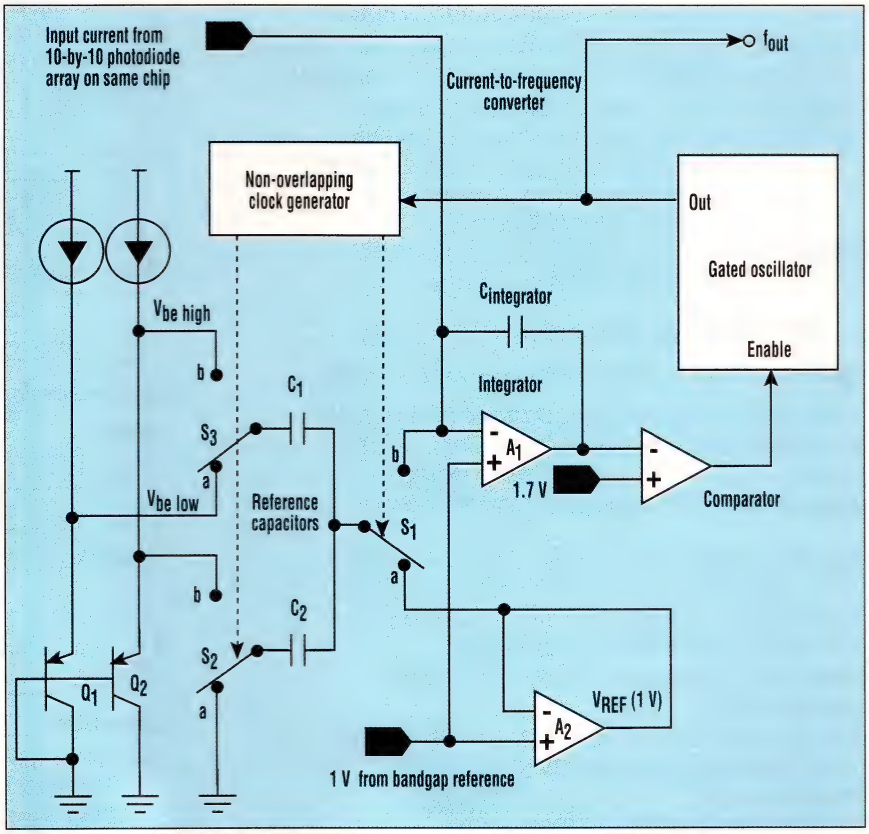
The 7-decade, light-intensity-sensing chip designed by a team from Texas Instruments, Dallas, contains a 10-by-10 array of 100 photodiodes *(Fig. 1)*. Each diode produces 4 μA for an irradiance of 100 mW/cm^2 at a wavelength of 660 nm. However, it's useful over a wavelength range of 300 to 1000 nm with only a small drop in sensitivity from its peak at 660 nm within the 300-to-1000-nm band.

Pin-strapping selects the use of 1, 10, or all 100 diodes to change the full-scale sensitivity. The array drives an integrating charge-to-current converter (CIC) circuit, which in turn drives a charge-balance current-to-frequency converter (IFC) circuit with a full-scale output frequency of 0.5 or 1 MHz and a 4-decade dynamic range *(Fig. 2)*. Thus, the chip handles a 7-decade range of light intensity—3 decades by pin-strapping and 4 with the IFC. At full-scale output frequencies of 0.5 MHz and 1 MHz, the IFC's linearity measures 0.2% and 1%, respectively.

The CIC circuit isolates the diodes from the IFC circuit, keeps them biased near zero so they can be used in the active photovoltaic mode, and provides a high-impedance (it's a current source) low-capacitance drive for the IFC circuit. The integrating CIC circuit transfers the light-generated charge on the diode's own shunt capacitance to a current.

For each cycle of the gated oscillator, the IFC switches capacitors C_1 and C_2 with MOSFETs S_1, S_2, and S_3 so that a fixed charge can be metered onto the circuit's integrating capacitor (C_{int}). Op amps A_1 and A_2 are identical, therefore the voltage at their summing nodes (–inputs) is nominally 1 V. Thus, as shown in the figure, reference capacitors C_1 and C_2 charge to voltages V_{REF} and $V_{REF} - V_{be\ low}$, respectively.

As A_1 integrates the current from the CIC, A_1's output voltage rises. When it reaches the reference voltage on the comparator's minus pin



2. CHARGE-BALANCING SWITCHED-CAPACITOR circuitry and integrator A_1 in the Texas Instruments IC convert the current from an on-chip 10-by-10 photodiode array to a frequency between 1 kHz and 1 MHz.

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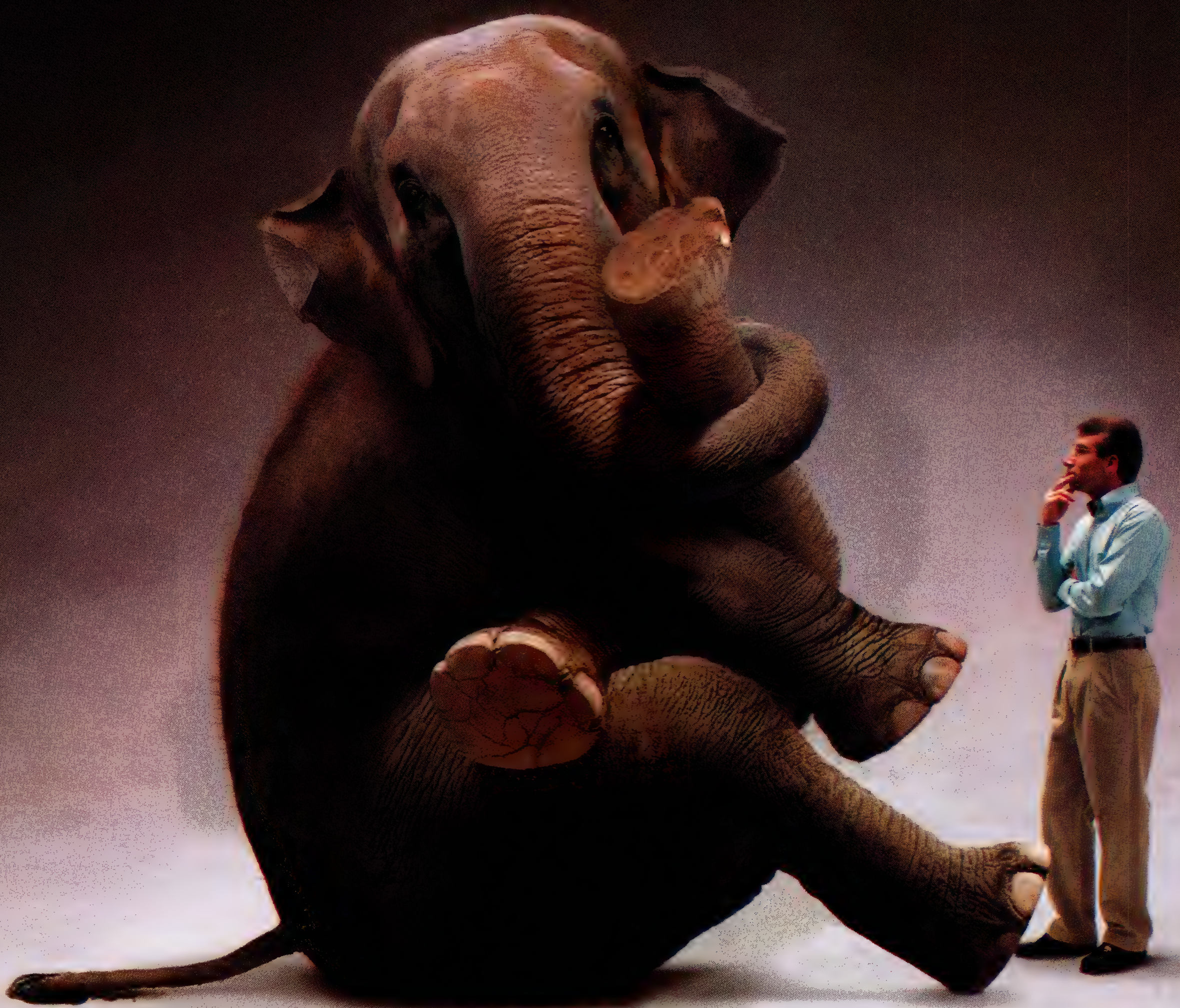

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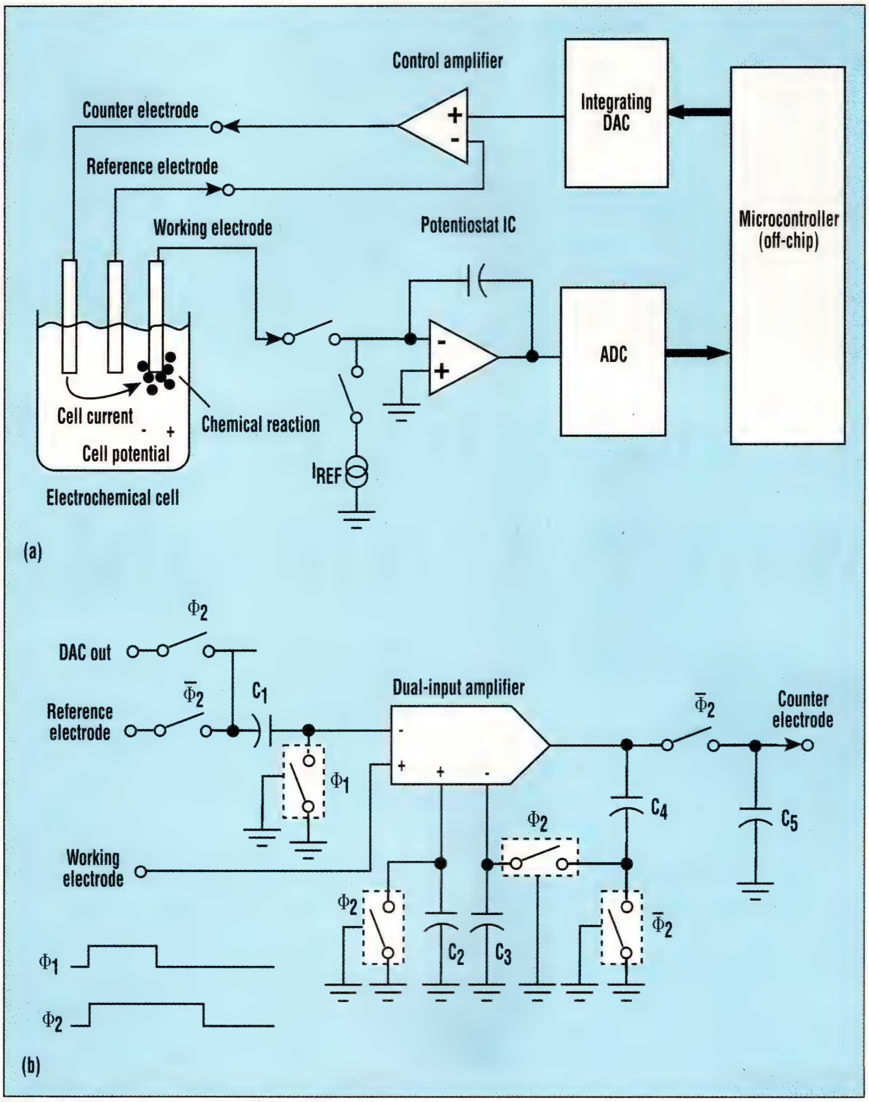
(1.7 V), the comparator's output goes high. This action enables the gated oscillator, which feeds a pulse to the output and toggles the three FET switches from a to b. S_1 switches the common connection of the reference capacitors from the 1-V dc reference voltage (V_1 to the minus input of the integrator, or A_1). S_2 switches C_1 from ground to $V_{be\ high}$, and S_3 switches C_2 from $V_{be\ low}$ to $V_{be\ high}$. This switch action delivers a charge (of value Q) to the integrator where (assuming complete discharge of the capacitors):

$$Q = C_1 \times V_{be\ high} + C_2(V_{be\ high} - V_{be\ low})$$

After approximately 320 ns, the oscillator's output changes state, returning the MOSFET switches to their original position and connecting the reference capacitors to their reference voltages (across the current-mirror npn transistors Q_1 and Q_2). Then the reference capacitors begin charging for the next cycle.

The charge transferred to the integrator is of the opposite polarity to that coming from the photodiodes. Consequently, it lowers the integrator's output voltage. The comparator-circuit's output then goes low, thereby gating the oscillator off until enough photocurrent is integrated to repeat the cycle. It's a closed-loop system, so the charge delivered by the reference capacitors balances the photocurrent, in turn creating an output frequency that's a log-linear function of the photocurrent.



3. THIS IC POTENTIOSTAT defines the voltage difference between two electrodes in an electrochemical cell (a). Current is measured through the cell caused by the chemical reaction within it. The control amplifier uses dual inputs to minimize the effects of charge injection in its switched-capacitor circuitry (b).

A POTENTIOSTAT IC

Large and expensive, power-hungry, bench-type instruments called potentiostats perform chemical analysis of samples of industrial, biological, environmental, and other materials. As an alternative, a three-man team, two from Stanford University in California and one from Tufts University, Medford, Mass., came up with a single CMOS chip that along with a microcontroller challenges the commercial laboratory instruments.

A potentiostat consists of a circuit/system that regulates the voltages on the electrodes in an electrochemical cell and then measures the current resulting from the chemical reaction it causes *(Fig. 3a)*. The potentiostat IC's integrating DAC (driven by the microcontroller) defines the voltage between the working electrode (where the electrochemical reactions of interest are taking place), and a chemically stable reference electrode. The control amplifier regulates this voltage by using feedback to drive a third electrode called the counter electrode. The current passing through the working electrode is measured with a current-input, dual-slope ADC.

The designers employed precision switched-capacitor techniques throughout the chip to cancel offset voltages and minimize charge-injection errors *(Fig. 3b)*. For example, in the dual-input control amplifier, the desired cell voltage (from the DAC) is sampled on C_1 while the amplifier's offset and charge-injection error is stored on C_3. These errors are sampled at a second, desensitized amplifier input to minimize charge-injection errors. A non-return-to-zero technique at the desensitized input keeps the amplifier from slewing to ground when sampling the offset. The amplifier's minus inputs operate at virtual grounds, eliminating bias voltages across critical junctions, which in turn removes virtually all leakage currents. The amplifier's plus input connects to the working electrode instead of ground, cancelling errors resulting from the elec-

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trode not being precisely at ground.

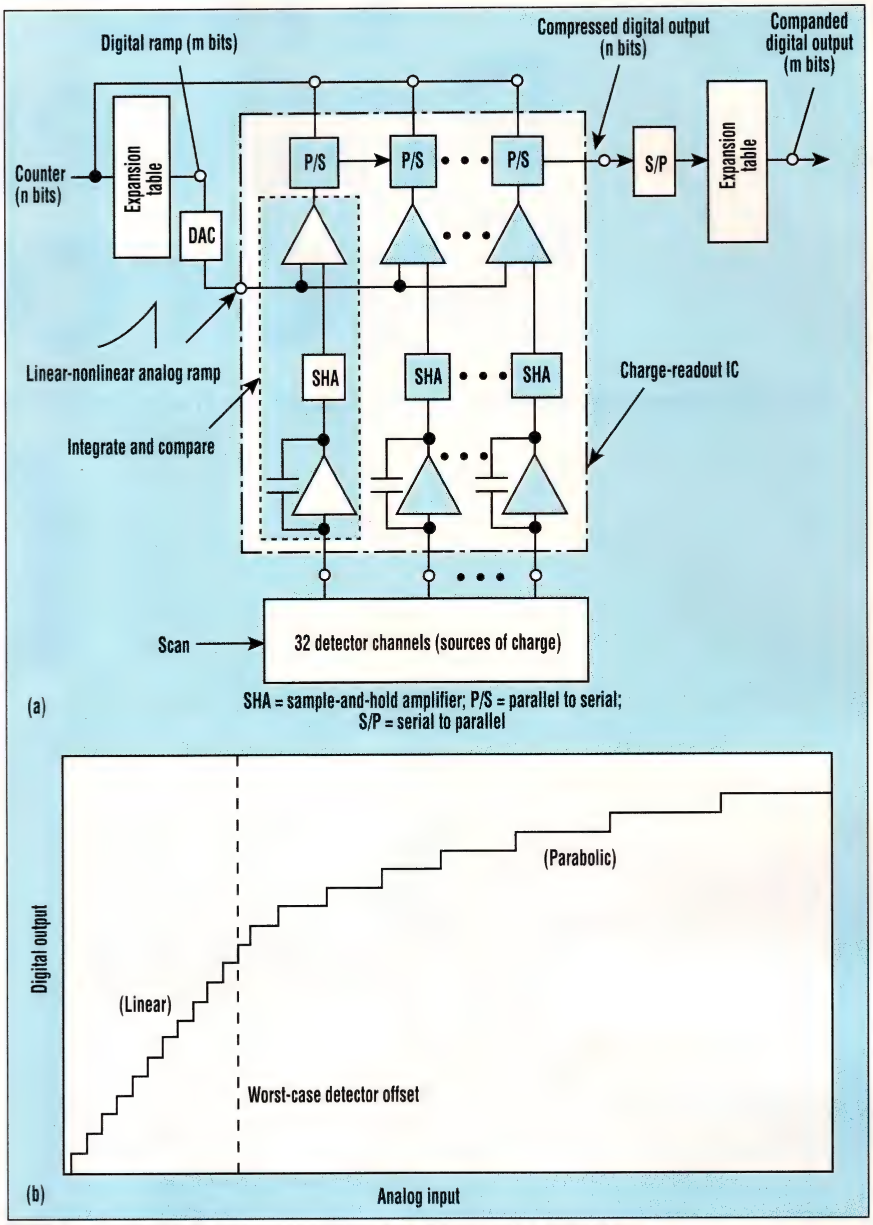
The autoscaling, current-integrating ADC handles currents ranging from 100 fA to 40 μA, providing 13-bit resolution and an accuracy of 0.02% of range. The DAC and control amplifier have a similar resolution and linearity for an input range from –4.8 to +4.8 V. In a typical commercial instrument, the EG&G 273A, the DAC has a range of ±8 V and 14-bit resolution. The ADC's current range runs from 2 pA to 1 A and accuracy is 0.5% of range. It weighs in at 31 kg and uses 350 W of power. The potentiostat chip takes just 5 mW.

CHARGE CHIP

Medical imagers also had a presence at the ISSCC. Developers of such imagers are consistently searching for and implementing the latest in analog technology. For example, most hospitals are now equipped with expensive but essential CAT scanner, which must integrate, sample, and quantize charge from hundreds of photodiodes.

Each photodiode receives inputs from a scintillation crystal being excited by X-rays. The dynamic range of the input usually approaches 1,000,000 to 1 (120 dB/20 bits). At present, most systems employ some form of integrating charge-to-voltage-converter-IC per channel followed (for reasons of cost and power dissipation) by a single, high-speed multiplexer and a high-speed (> 100 kHz), high-resolution (16-bit) ADC. However, every system designer would like to replace the multiplexer and single ADC with an ADC/channel followed by a digital multiplexer. Many detectors used in high-energy particle physics systems require similar data-acquisition systems.

Addressing this situation, a multidisciplinary team from Case Western Reserve University, Cleveland, Ohio, General Electric Medical Systems, Waukesha, Wis., and the General Electric Corporate R&D Center, Schenectady, N. Y., developed a single CMOS IC that handles 32 sources of charge. It provides a digital output for all 32 channels (with 17 bits of dynamic range) every 50 μs and consumes just 15 mW/channel *(Fig. 4a)*. The designers call it a charge-readout integrated circuit, or CRIC.


Digital ramp (m bits)
Compressed digital output (n bits)
Companded digital output (m bits)
Counter (n bits)
Expansion table
DAC
P/S
P/S
P/S
S/P
Expansion table
Linear-nonlinear analog ramp
Integrate and compare
SHA
SHA
SHA
Charge-readout IC
Scan
32 detector channels (sources of charge)
(a)
SHA = sample-and-hold amplifier; P/S = parallel to serial; S/P = serial to parallel
(Parabolic)
Digital output
(Linear)
Worst-case detector offset
(b)
Analog input

4. A SINGLE CHIP SAMPLES AND QUANTIZES 32 channels of charge-sourcing detectors for a medical-imaging application while offering 17 bits of dynamic range (a). A nonlinear ramp stored in off-chip memory (an expansion table) provides compression to achieve the dynamic range (b).

Because dynamic range is more important than absolute accuracy in these applications, the chip combines an arbitrary and nonlinear quantization (data compression) technique with integrate-hold-and-compare circuits that double-sample the charge on the detector's capacitors. The compression curve is tailored to match the detector's noise characteristics. Square-root companding doesn't solve the problem because the detector can have a random offset greater than that produced by a minimum detectable unit of charge, or one quantum. Instead, signals falling below the maximum expected offset are quantized linearly with a resolution of one quantum. Signals greater than the expected offset are quantized against a parabolic reference. The compression curve differs according to the gain range, but less than 350 quantization levels are needed to span a 13-bit range if the minimum cycle time is 50 μs.

The programmable compression curve is stored in off-chip digital

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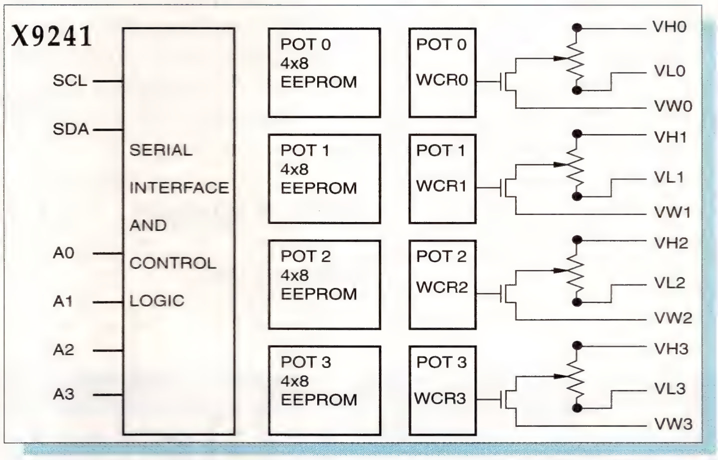
Design Engineers Bulletin

New Product and Applications Information for Design Engineers

Xicor's New X9241 Quad Potentiometer Allows Factory Automation of 64 Potentiometer Adjustments via a Digital Two Wire Serial Bus

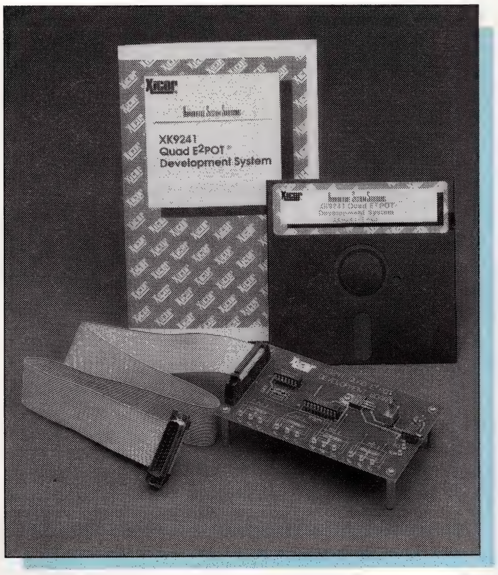
For complex systems requiring multiple adjustment capability, Xicor offers the new X9241, Quad E^{2}POT. In addition to retaining wiper positions without power, the X9241 offers a two-wire serial interface for controlling the potentiometers independently or simultaneously using microprocessor control commands. A user programmable address allows up to 16 devices to be software controlled via the common two wire serial bus.



Data Sheet Enclosed

Quad E^{2}POT Development System

PC based system automates production adjustments of system potentiometers



The XK9241 can be used in a production environment to optimize the settings of the E^{2}POT.

Faster analog circuit checkout and calibration is made possible by Xicor's new XK9241W Quad E^{2}POT Development System. This system consists of an X9241 evaluation board, interface cables and software which allows a design engineer to control all functions of the Xicor X9241 Quad E^{2}POT from a menu driven system on a IBM PC Compatible computer. The XK9241W Development System allows the design engineer to place the X9241 in a target analog system and perform all adjustments and configuration needed to recognize the features and benefits of the Quad E^{2}POT.

The XK9241 PC based development system can also be used in production environments to automate potentiometer adjustments for initial system calibration.

The XK9241 supports all versions of the X9241 family. It can simultaneously control up to 16 different Quad E^{2}POTs on the same two-wire bus to effectively allow adjustment of 64 individual E^{2}POTs. Orders for the XK9241W can be placed with any authorized Xicor distributor. Suggested resale price is $180.00.

Data Sheet Enclosed

Xicor Inc., 1511 Buckeye Drive, Milpitas, California, 95035 Telephone (408) 432-8888 Fax (408) 432-0640

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memory (a lookup table) *(Fig. 4b)*, where it's easily changed to meet the characteristics of the detector. An off-chip DAC converts the curve to analog form. For systems with more than 32 channels, both the memory and DAC can be shared by multiple CRICs. The architecture combines the benefits of an ADC/channel with the power consumption of an analog charge-to-voltage converter, followed by a multiplexer and an ADC.

During conversion, a counter drives the off-chip expansion table, which has stored the reciprocal of the compression curve. This creates a digital ramp that's applied to the DAC to produce an analog ramp. This ramp is simultaneously compared to the outputs of every sample-and-hold amplifier (SHA), which are actually sampling comparators. When each comparator trips, the counter value at that time is latched and held by a parallel-to-serial (P/S) converter. At the end of each set of conversions, the compressed digital data from a group of channels is shifted out for conversion to a parallel format and then expanded using an identical expansion table.

The integrate-and-compare circuitry consists of three switched-capacitor amplifier stages: the integrator, a double-sampling amplifier, and a SHA. The detector (a source of charge) output is switched to its 100-pF parasitic shunt capacitance when "Scan" is high. The integrator converts this charge to a voltage. The double-sampling amplifier performs a low-pass filter action on the voltage and amplifies the difference in the filtered voltage before and after "Scan" is applied. Its output is applied to the sampling comparator and compared to the analog ramp.☐

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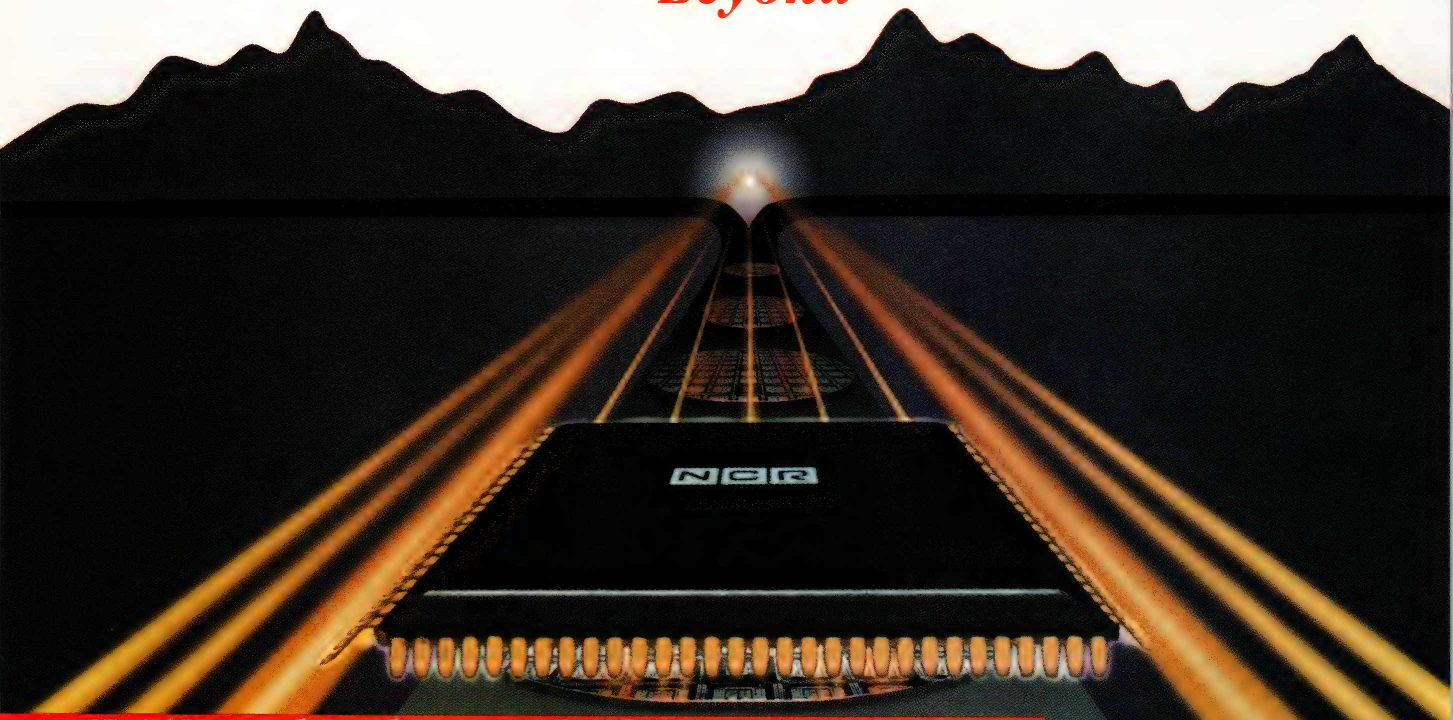

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521 INDUSTRIAL F/V CONVERTER

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C.J. Controls Ltd., Penclawdd Industrial Estate, Penclawdd, Swansea, England
SA4 3RS; Tel.: (0792) 851083, Fax: (0792) 850442.

Control and process equipment often require the indication of frequency (speed or rate) of linear or rotary mechanical movement. Motion can be detected using various pulse-generating pickups and proximity detectors that output ac or dc pulsed signals. Microprocessors or dedicated frequency-to-voltage converters may be employed in counting and processing the signals. Most of the time, however, the need arises to simply and inexpensively convert the frequency into a usable dc voltage.

This industrial converter *(see the figure)* can serve in a wide variety of applications. In fact, it's now used in a number of standalone displays as well as in open- and closed-loop systems (for example, in the display of the rate of bottles passing on a conveyor; as a liquid flow feedback signal from a vane sensor; and to indicate the speed of a motor using a toothed wheel sensor).

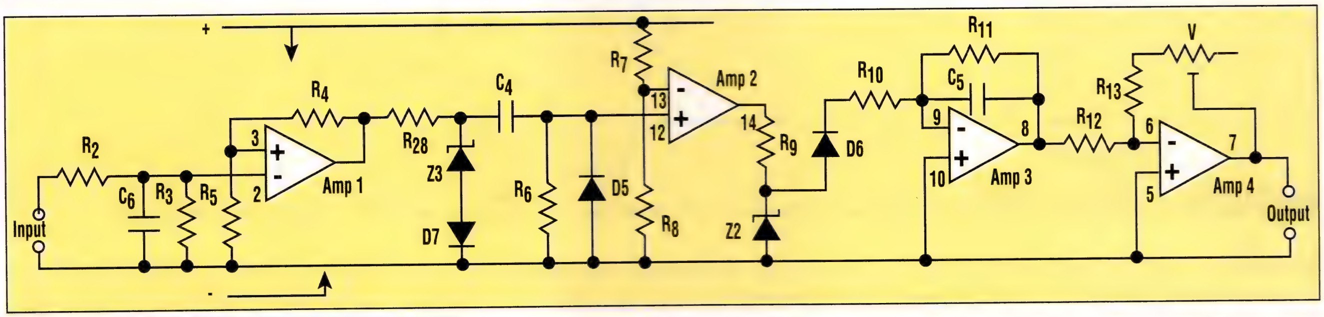
The circuit operates around a quad-FET input op amp and is designed to be self-contained or run from a bipolar supply. The input signal of dc pulses or ac waveforms is applied to R_2.

Amplifier 1, which acts as a Schmitt trigger, supplies a square-wave output of fixed amplitude to C_4. Resistor R_3 and capacitor C_6 filter out input noise, while R_4 and R_5 determine the switching levels, and zener diode Z3 sets the amplitude.

Amplifier 2 gives a fixed duration pulse on the positive transition of C_4, with a time constant set by C_4 and R_6 and the switching level set by R_7 and R_8. Resistor R_9 and zener diode Z2 fix the amplitude of the pulses and amplifier 3 integrates them via R_{10} and C_5. Diode D6 blocks negative integration and R_{11} discharges C_5 with a long time constant.

Hence, the dc output of amplifier 3 is proportional to the frequency applied to the input. Amplifier 4 inverts and buffers the negative output of amplifier 3 and provides amplitude adjustment voltage.

The complete circuit is linear and sufficiently accurate providing that C_4 is chosen to give a pulse duration less than the maximum input frequency and that $R_{11} >> R_{10}$.☐



THIS FREQUENCY-TO-VOLTAGE converter can be used in a variety of industrial applications, including standalone and open- and closed-loop systems.

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522 JITTERLESS 1-CYCLE F/V CONVERTER

W. STEPHEN WOODWARD and JOHN PETERSON
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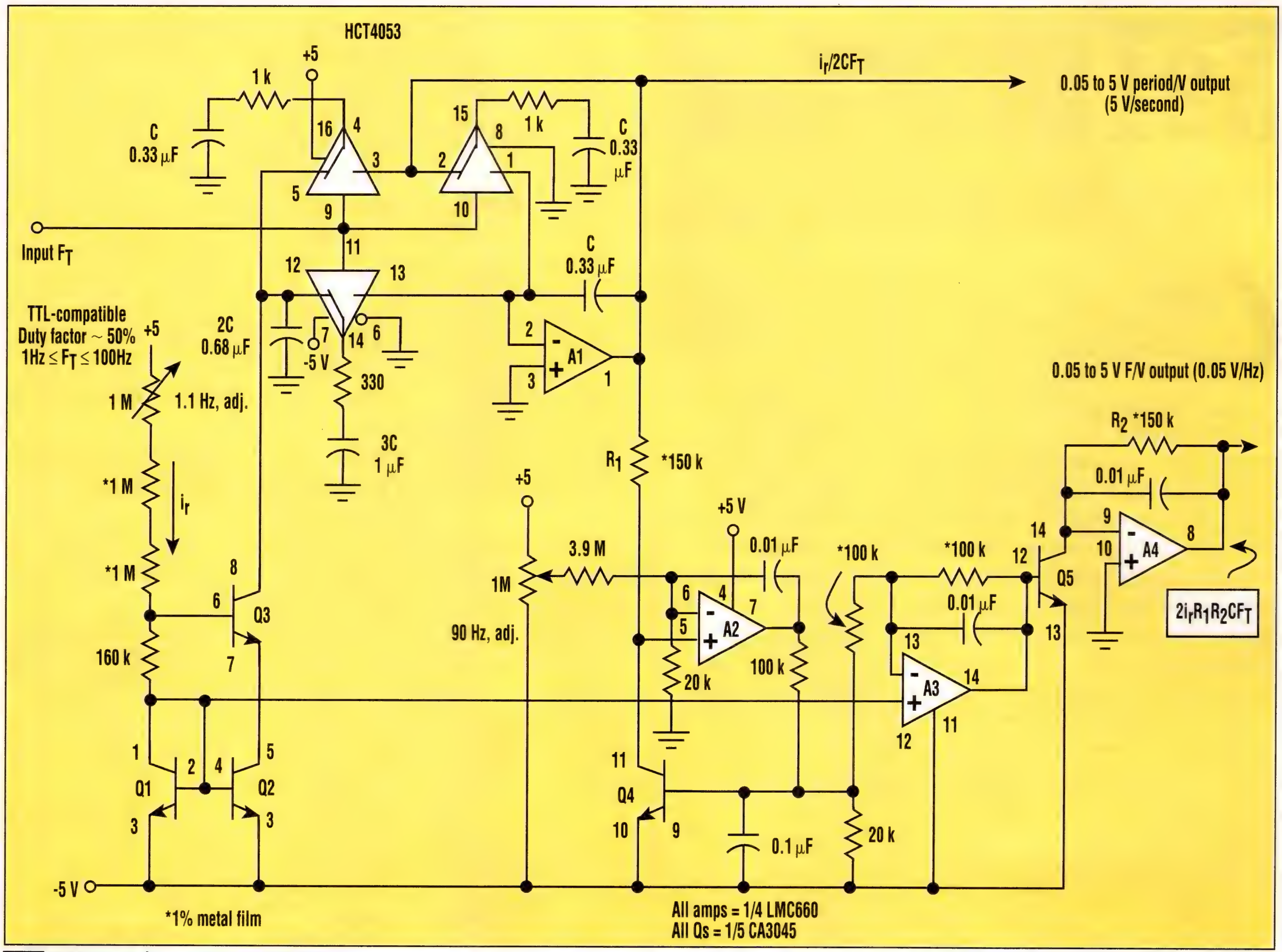
In Mr. Robert A. Pease's column "What's All This Frequency-to-Voltage Converter Stuff, Anyhow?" (ELECTRONIC DESIGN, *July 8, 1993, p. 81)*, he presented an elegant hybrid digital/analog frequency-to-voltage converter. The design used a 12-bit DAC in an unusual reciprocal-computing connection: It converted a 12-bit digital measurement of the input-signal period directly into a frequency-proportional analog output. The conversion result settled in only one cycle of the input signal.

An undesirable property of the converter, however, arises from the same digital measurement technique that makes single-cycle settling possible. For input frequencies anywhere near the full scale of the converter, the finite clock frequency (32768 Hz) used to drive the period-measuring counter causes a noticeable ±1/2-bit jitter in the output.

This limitation is avoidable by im-



THIS F/V CONVERTER employs an analog integrator to measure the input signal period, thus avoiding jitter in the output.

plementing an analog integrator to measure the input-signal period *(see the figure)*. The Q1, Q2, and Q3 elements of a CA3045 transistor array serve to generate a $\approx$3.3-μA reference current (i_r) that controls a timing ramp at the Q3, C_1 node. This ramp is sampled and reset once every cycle of T (the TTL-compatible input frequency) by the combination of HCT4053 CMOS switches and A1 (1/4 of an LMC660 quad op amp). The resulting samples are held on the output of A1 and made available as a direct readout of the period of T equal to: $i_r/2C/F_T$, where F_T is the frequency of the input signal. In the example circuit, the $i_r/2C$ scale factor has the value of 5 V/second. Consequently, periods of up to 1 second can be handled without overrange thanks to the rail-to-rail output of amplifier A1.

The period readout voltage generates a current through the scaling resistor R_1, which serves as an input to an analog reciprocal-computing circuit formed by Q4, Q5, A2, A3, and A4. A4's output voltage is given by: $2i_rR_1R_2CF_T$. Because A4's scale factor in the example circuit is 0.05 V/Hz, frequencies up to 100 Hz can be accurately converted to a 0-to-5-V output span.

The "1.1 Hz" trimpot sets i_r and, therefore, the bottom end of the F/V conversion span. The trimpot labeled "90 Hz" compensates the zero offset of the reciprocal-circuit input amp, thus optimizing the linearity of the upper end of the F/V span. If independent calibration of the period and frequency readouts is desired, R_2 can optionally be made variable and used for the 1.1 Hz adjustment. The "1.1 Hz" trimpot is then reserved for tweaking of the period-dependent output.☐

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TELEPHONE RING GENERATOR

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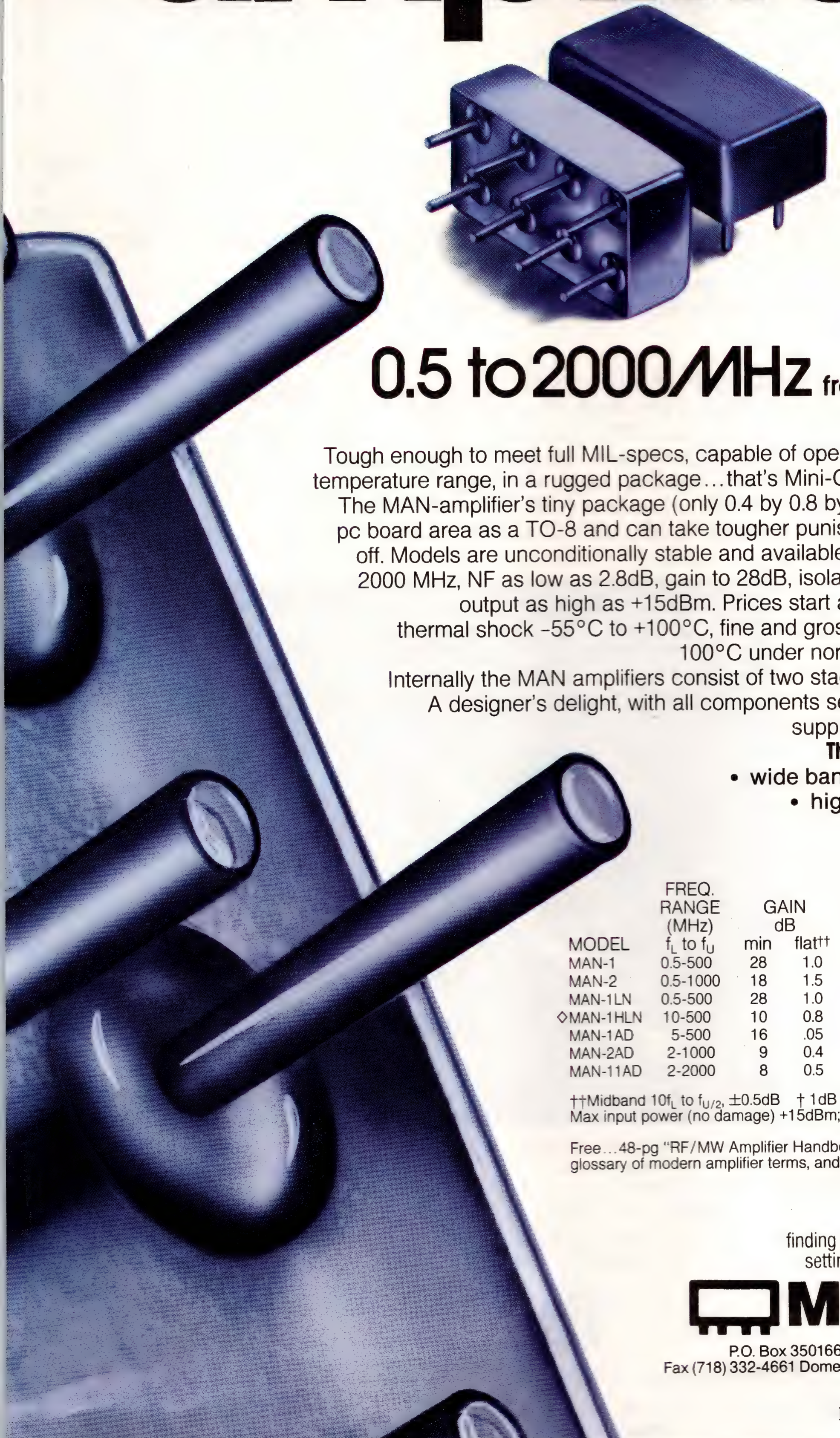
Many telephone accessories simulate a central office (CO) by ringing or supplying power ("Battery") to a telephone. Examples of such products are fax switches, PBXs, or phone-line switchers.

This circuit *(see the figure)* uses inexpensive, commonly available components to generate a telephone ring

rugged plug-in amplifiers



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◇MAN-1HLN	10-500	10	0.8	+15	3.7	14	12/70	15.95
MAN-1AD	5-500	16	.05	+6	7.2	41	12/85	24.95
MAN-2AD	2-1000	9	0.4	-2	6.5	28	15/22	22.50
MAN-11AD	2-2000	8	0.5	-3.5	6.5	22	15/22	29.95

††Midband $10f_L$ to $f_{U/2}$, ±0.5dB † 1dB Gain Compression ◇Case Height 0.3 in.
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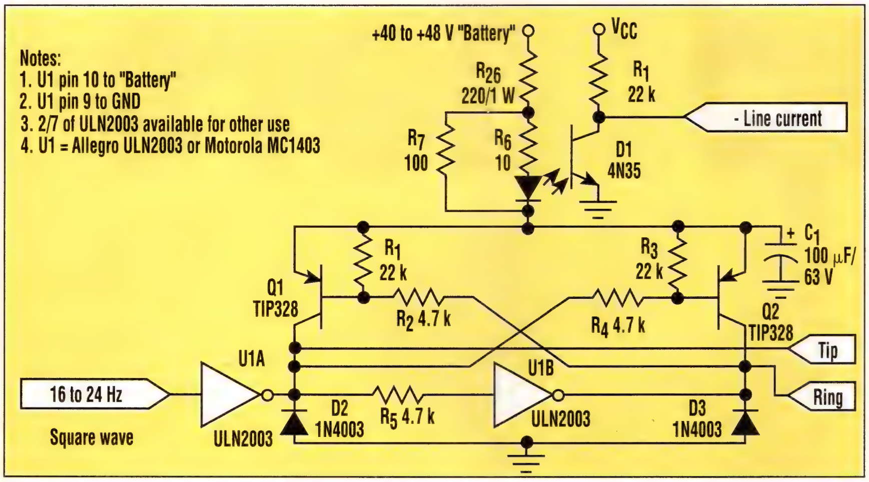

A TELEPHONE RING SIGNAL can be generated using this circuit made up of inexpensive, common components. A switchable polarity "Battery" also can be supplied to the telephone.

signal as well as supply a switchable polarity "Battery" to a telephone.

With a high input, the output of the open-collector driver U1A ("Tip") is low. Current flows through R_4, turning transistor Q2 on and pulling "Ring" high. Both U2A and transistor Q1 are off.

With a low input, Tip is high and Q2 is off. The output of U2A ("Ring") is low. Current flows through R_2, forcing Q1 on. Optoisolator D1 turns on once the phone is picked up. The 48-V "Battery" supply may be generated from a low-voltage ac wall-plug transformer using a voltage doubler or tripler.

A microprocessor output or 555 timer can generate the 16-to-24-Hz source, so long as it provides an approximate square wave. Once the controller detects that the phone has been picked up, it turns off the square wave and either +48 V or –48 V is supplied to the phone.

In other applications, the output polarity may be momentarily switched to simulate a central office "wink start" upon detection of line current.☐

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Charles Hartley, P.O. Box 614, San Carlos, CA 94070. His idea: *"Simple RS232 Sync To Async Converter."*

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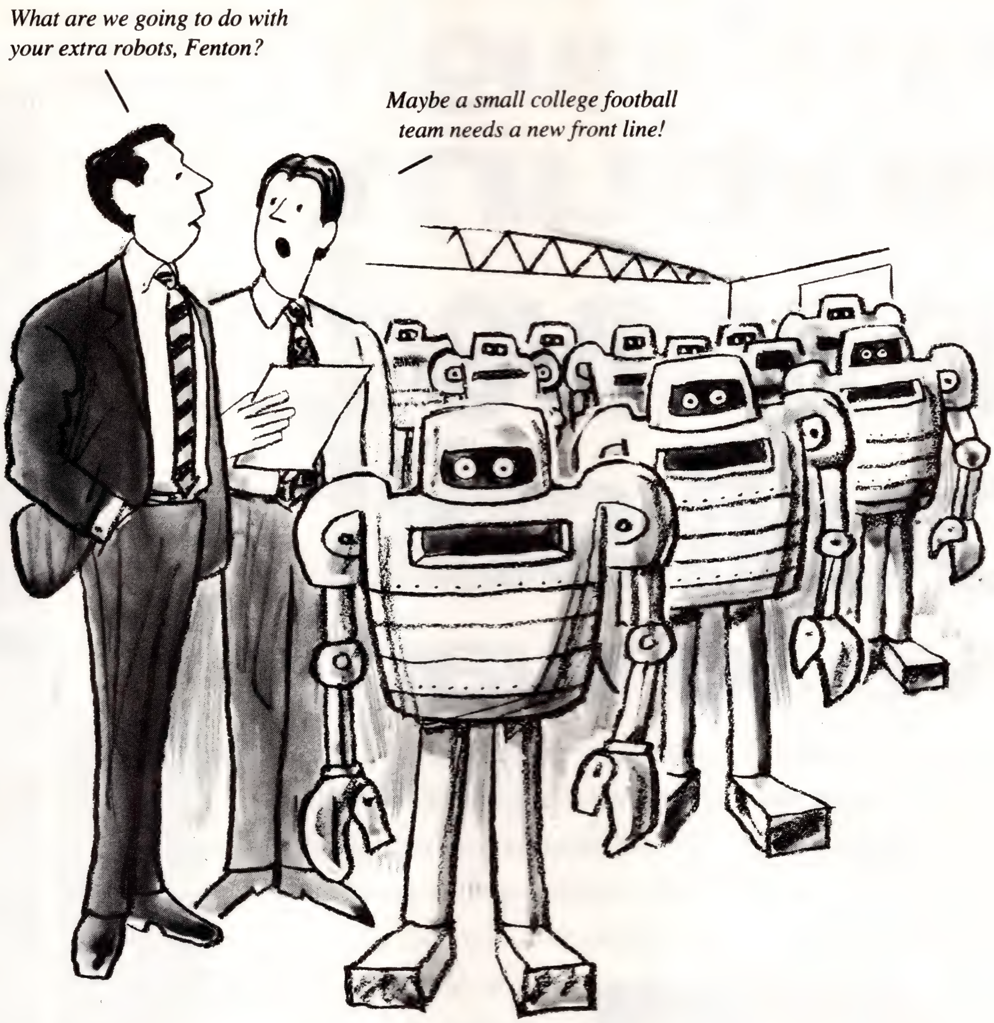
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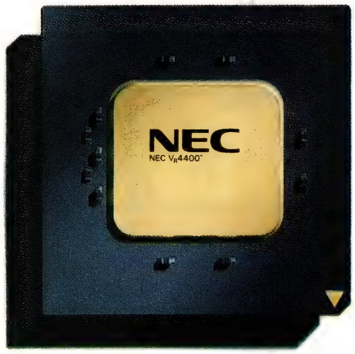
Our V_R4400™ 150MHz microprocessor runs Windows NT* nearly twice as fast. Not marginally faster. Not even quite a bit faster. Nearly twice as fast. And we have them ready and waiting to speed you into the future.



The NEC V_R-Series processors come in a variety of scalable performance/price configurations–many of which are significantly less expensive than Pentium.

None of this should be surprising, really. Not when you consider that our processor is already at the heart of the most powerful workstations in the world.

You see, NEC's V_R-Series is based on MIPS Technologies'® 64-bit RISC architecture. And now, that same workstation performance is available for desktop PCs running Windows NT. In fact, Windows NT was developed on our processor.

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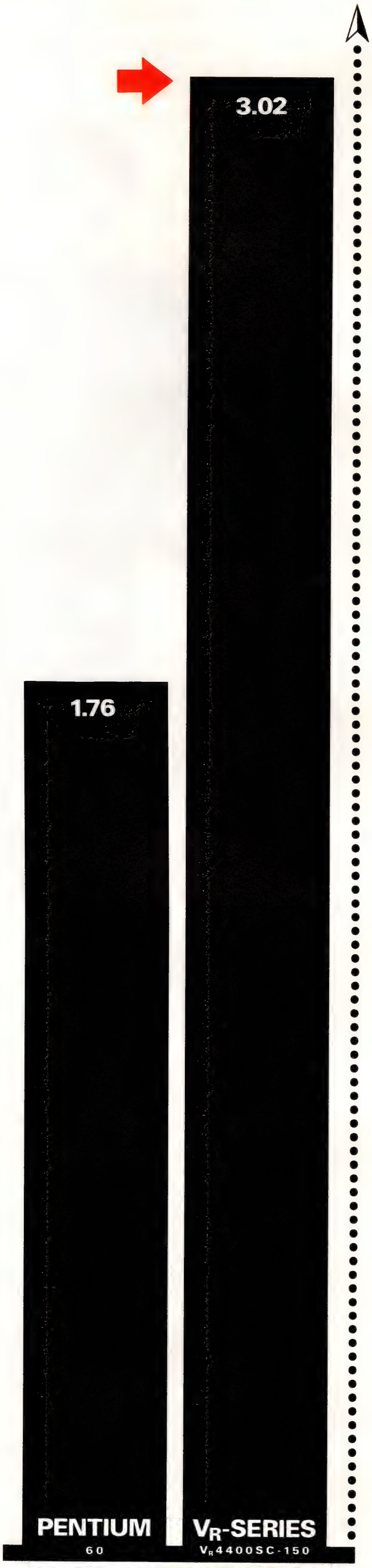

BYTE BENCHMARK
PERFORMANCE RELATIVE TO 486-66

NEC

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ELECTRONIC DESIGN QUICK LOOK

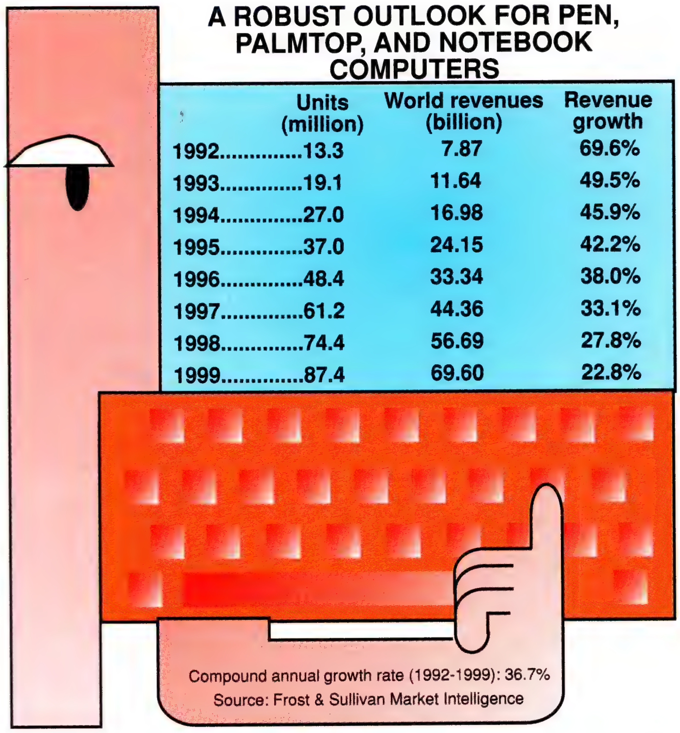
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Global sales of sublaptop computers and peripherals are expected to grow robustly, increasing from $11.64 million last year and projected to reach $69.20 million by 1999. That's the forecast of a new study by Frost & Sullivan Market Intelligence.

The most rapidly growing segment is that for pen computers, which enable users to enter data with a penlike stylus instead of a keyboard. Sales of these units are expected to grow at a 68% compound annual rate, increasing from 4% of the total worldwide market for sublaptops in 1992 to 16% by 1999. Notebook computers will hold their own, accounting for two-thirds of revenues for compact units throughout the decade, according to the Mountain View, Calif., company's report, *World Pen, Palmtop and Notebook Computer and Peripheral Market: Solid Profits in Accessories, but Will PDAs Follow?*

Pen technology is working its way into a growing diversity of products. Personal digital assistants (PDAs) rely on pen software applications and communication features. Hybrid pen/tablet notebook computers bundled with pen-based personal information management (PIM) software may well attract users of notebooks. Some palmtop computers, like Sharp's Wizard, enable users to enter data with a stylus or with a keyboard.



A ROBUST OUTLOOK FOR PEN, PALMTOP, AND NOTEBOOK COMPUTERS

	Units (million)	World revenues (billion)	Revenue growth
1992	13.3	7.87	69.6%
1993	19.1	11.64	49.5%
1994	27.0	16.98	45.9%
1995	37.0	24.15	42.2%
1996	48.4	33.34	38.0%
1997	61.2	44.36	33.1%
1998	74.4	56.69	27.8%
1999	87.4	69.60	22.8%

Compound annual growth rate (1992-1999): 36.7%

Source: Frost & Sullivan Market Intelligence

TALES FROM A SKUNK WORKS

OK, Trudel we read your column faithfully and we believe in skunk works and innovation. So tell us how to get started.

The first step is ensuring top management understanding and support. I'd state it as something like, "With a few notable exceptions, most Western firms are losing at technology-based products. We can win, but it will require major changes. Improving new product development is crucial." Unfortunately, most of the upper managers I have spoken with in the U. S. don't see things that way.

Some don't know that we are losing while others are convinced they can't win at products. Some take criticism personally and attribute 20 years of layoffs and market share loss to "the recession." This is similar to U. S. problems in education. Tell a school official that her K-12 students score near the bottom of the industrialized world, and she will become defensive. Like U. S. managers, some educators have data that proves all is well. Others agree that things are bad but feel helpless and are powerless to act.

The U. S. K-12 system is producing better students than ever before. U.S. firms are producing better products. The problem is that slowly and inexorably, our business methods and models have become outdated. *Relative to our competition, we lag.*

Western management and political sensors are short-term and event-based. If someone burns our plants or bombs our cities, we take note. But we don't notice the slow systemic changes that are the biggest threats to our existence. This is the frog-in-a-pot problem.

Put frog A into a pot of room-temperature water. It will swim happily. Drop frog B into a scalding pot, and it will flee. But put frog C into a pot of water and place the pot on a burner, and the frog will slowly cook to death. By the time the frog senses that its comfortable environment has turned lethal, it can't escape.

Your goal is to inspire major change without being fired. Don't dismiss barriers as simple reluctance to change. Social systems—including successful corporations—work very hard to survive. Often at great cost, they maintain their boundaries, work methods, and patterns of interaction. The more you push, the more they resist. You won't win such a struggle.

When your top management truly believes that new product development is crucial and that major improvements are needed, proceed. Get seed money, retain a mentor who has been through this often and start work. Most firms aren't yet ready for this step.

If top management does not truly perceive this opportunity as crucial, then it is best to wait. Don't push, educate. My next column discusses education and development of shared vision.

John D. Trudel CMC, CPC, is a management consultant from Scappoose, Ore.: <johntrudel@aol.com>

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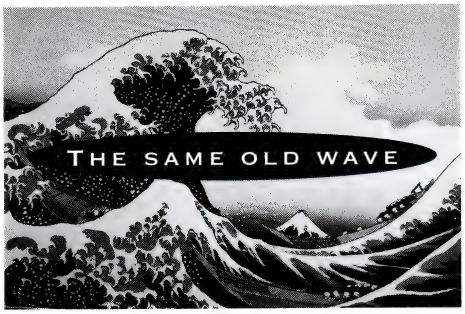

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A dictionary of terms and definitions for fiber-optic communications is free from Methode Electronics Inc.'s Fiber Optic Products Div. The pocket size, 62-page dictionary defines such terms as deterministic jitter, quantum efficiency, and loose-tube buffering. For a copy, contact Methode Electronics Inc., Fiber Optic Products Div., 7444 W. Wilson Ave., Chicago, IL 60656; (800) 323-6858 or (708) 867-9600; fax -9130. CIRCLE 461

A book of application notes on MMICAD, Optotek's RF and microwave CAE and CAT software for DOS and Windows, covers MIC and MMIC design topics including filters, amplifiers, oscillators, switches, and data acquisition from network analyzers. *MMICAD Application Notes* is available for $20 US. Contact Dave Girard, Optotek Ltd., 62 Steacie Dr., Kanata, Ontario, Canada K2K 2A9; (800) 361-2911; (613) 591-0336; fax -0584. CIRCLE 462

More than 1900 U. S. government laboratory and information centers are described in the 5th edition of the *Directory of Federal Laboratory & Technology Resources—A Guide to Services, Facilities, and Expertise.* The directory, organized in 72 subjects and indexed by state, organization name, and government agency, is published by the U.S. Department of Commerce's National Technical Information Service (NTIS) and the National Technology Transfer Center. The 736-page directory is $65, plus $3 shipping and handling, from NTIS, order no. PB93-10009KSZ; (703) 487-4650; fax (703) 321-8547.

Copies of TIA/EIA standards documents for fiber optic cables are available at low cost. For example, document TIA/EIA-455-41A, FOTP-41 Compressive Loading Resistance of Fiber Optic Cables discusses tests determining the ability of fiber-optic cable to mechanically and optically withstand or recover from the effects of compressive force, slowly applied. Available separately at similar costs and from the same address, other documents cover such topics as data transmission systems and equipment, electrical characteristics for an interface signalling at up to 52 Mbits/s, and visual and mechanical inspection of multilayer ceramic chip capacitors. Copies of the fiber-optic document are $28 each from Global Engineering Documents, 15 Inverness Way E, Englewood, CO 80112-5704; (800) 854-7179; (303) 397-7956.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (408) 446-4458; fax (408) 253-6085

He who labors diligently need never despair; for all things are accomplished by diligence and labor.
—Menander of Athens

Attention has been focused on the denominator of the work quantity /commitment = duration equation. In this column, producing the numbers associated with the numerator—work quantity—are explored.

First, it's important to identify the information source for work quantity estimates. Do they come from executive managers, project managers, team leaders, or team members?

To answer the question, let's develop a scenario that an engineering group might encounter. For example, suppose an ASIC has to be developed for a new telecommunication product. The functions that the ASIC must perform are known and operating interfaces are well specified. In addition, a time-to-market target is already being discussed within the organization.

This time-to-market figure sets the stage for the desired duration of this ASIC's design and development. Where does the time-to-market information come from? Most of the time, I hear executive managers creating the initial numbers—these folks read my column; they know how important time to market is; and they know that less is better. To expect another response would be unreasonable! On the other hand, an organization cannot expect its executive management team to fully understand work detail. And the initial time to market figure being promoted may not be right. Developers must provide the balance.

To get the needed balance, new product development organizations often turn to their project managers and team leaders. These people have built a library of experience and have established a track record for making duration estimates within the product development environment. The estimation performance of this group, working independently, is usually quite flawed; few, if any, have good reputations for estimation accuracy. They tend to think in highly optimistic terms.

Often, events from the past are swept under the carpet or intellectually attacked and deemed insignificant. My list of the top 40 events that cause project delay is completely ignored by most who make estimates this way. And interestingly, the time numbers produced are often times very close to those initially stated by executive managers. To make good estimates, these folks need help. Where do they get it?

To get work quantity numbers right, team members, who have actually done similar work, need to be an integral part of the estimation process. Team members should know the number of hours that go into design; simulation; redesign; build; test; redesign; second build; and second test. They will know the number of design cycles needed to get an ASIC fully operational and into a product that is released to manufacturing.

They will know that use of similar processes and similar tools will produce similar results; and they will be able to quantify the work hours associated with each step along the way. Project managers, team leaders, and team members must agree on the approach and the desired outcome. As they do, the production of quality work-quantity figures associated with each step materializes.

So, how do you get good work quantity estimates? Team members do the initial production! Once this is done, the team members, team leader, and project manager work together to understand the assumptions that were made and to ensure the estimates are based on reality. A few iterations are likely to be needed to get it right, but once the process is complete, this data is used to clearly define how time-to-market goals can be realized.

More information on this topic is contained in New Product Development: Design and Analysis, which can be obtained by calling Time to Market Associates.

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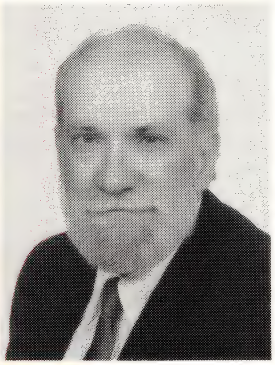
MY VIEW

...About getting it

BY FRANK J. BURGE
Director of Market Development for Electronic Design



A few months back I attended a company's annual stockholders meeting. After the meeting I asked a Wall Street analyst who follows the company what he thought about the presentation. He smiled: "They just don't get it." Later that same week I had breakfast with a marketing type from a major semiconductor company. We talked about his business and the challenge of trying to figure out which customers will be winners and which ones will likely finish out of the money.

When I asked why he put certain companies on his "out-of-the-money list," his eyes lit up: "They just don't get it." But getting it is what it is all about. Intel gets it; Motorola gets it; Hewlett-Packard gets it. Compaq didn't get it but gets it now. IBM and Digital didn't get it and are still figuring it out. One is closer to getting it than the other. In some companies the CEO gets it but the lieutenants don't. In others the lieutenants get it but the general doesn't.

Working for a company that gets it is usually more fun than working for one that doesn't. The companies that get it are market-driven, not product driven. As market leaders, they offer the most exciting product-development challenges with a market payout. Developing a product that the market votes a success just makes one feel good about being part of it all. And developing products the market wants has built-in job security. But there is something else. Developing products the market wants helps create and preserve a sense of family.

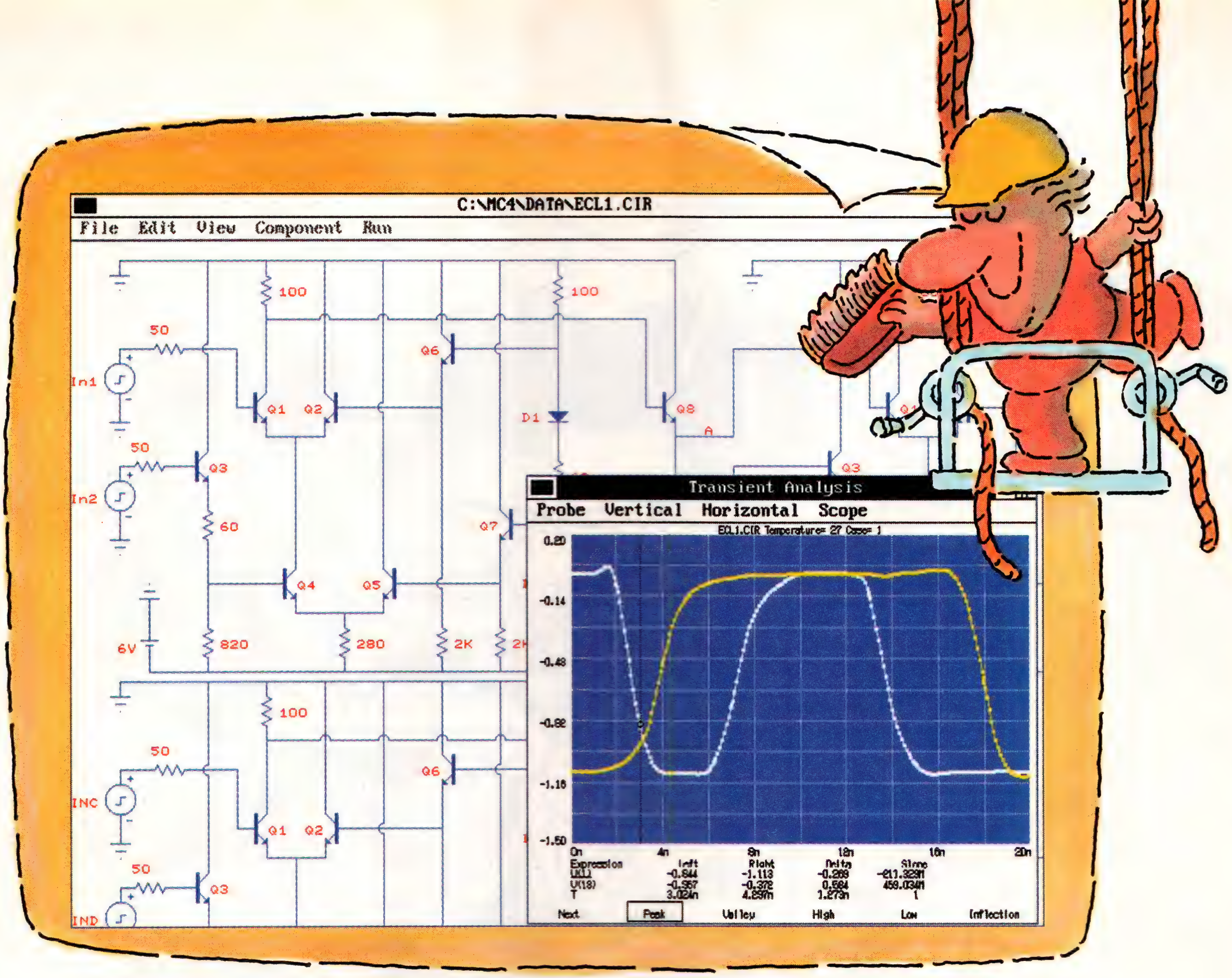
There was a time in business when there was a certain sense of job security, a sense of belonging. Going to work meant being with old friends, being with family. There were shared values and a sense of caring. The sense of family is something I experienced years ago at Beckman Instruments and Fairchild Semiconductor. And I'm sure it's the same good feeling the folks at Siemens, Toshiba, Samsung, Tektronix, and the Rock Island Railroad experienced—a warm, comfortable feeling of belonging, of being with people at work who were family. Now that's fun.

Then something happened that changed everything: competition. It came not just from across the street or down the road but from places whose names you couldn't pronounce. Competition from folks who looked different, talked different and who were out to eat your lunch in the marketplace. Competition has a way of threatening your job security.

Today more people are concerned about losing their jobs than at any time in my adult life. The traditional lifetime employment guarantee has become a relic of the past. When your buddy at work gets canned, it does something to your brain and you start looking over your shoulder and waiting for the next casualty of the downsizing landslide.

Something more sinister happens too—going to work isn't fun anymore. There is no longer an atmosphere of caring and sharing, a sense of family. Instead it's every person for himself. Keep your mouth shut. Play it close to the vest. Protect your buns. And your gut begins to ache.

So how do we shovel our way out of this mess? From my perch it looks as if there are three alternatives. If you're stuck in a company that doesn't get it, then cash in your chips and move on. Move on before you drown in a sea of self pity. Or you get tossed in the dumper as the company gets taken to the mat by the competition. Or you may decide to stick it out and become an agent of change. That's a tough assignment, particularly if the folks who run your company just don't get it. Shoveling against the tide is gut-wrenching work but filled with rewards if you pull it off. Then there is the third alternative—go into some other line of work. Get it?



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Expression        Left      Right     Delta       Slope
V(1)            -0.844     -1.113    -0.269   -211.329M
V(18)           -0.957     -0.372     0.584    459.034M
T               3.024n     4.297n    1.273n           1
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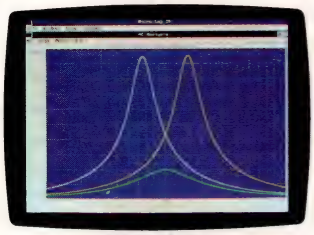

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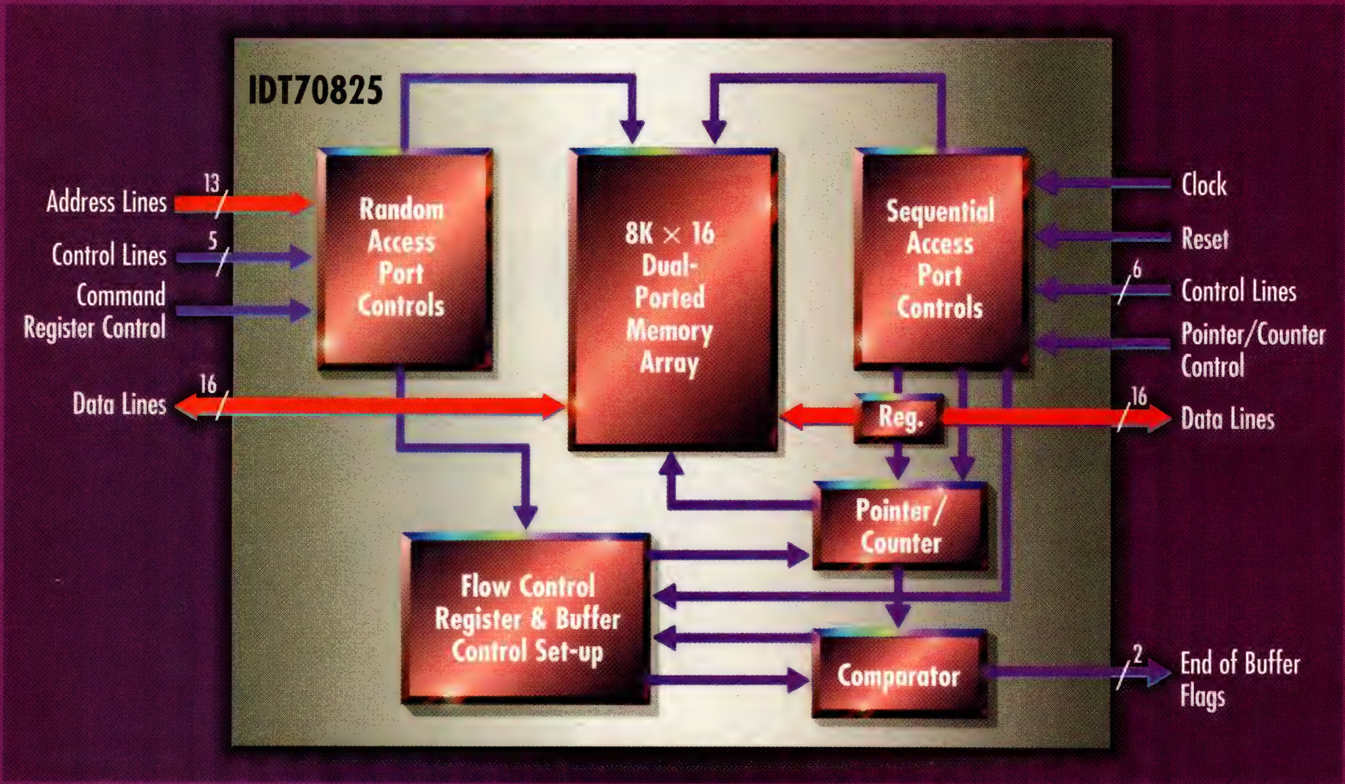

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PEASE PORRIDGE

BOB'S MAILBOX

Dear Bob:

I have as usual just read with pleasure your Dec. 16, 1993 article concerning "Floobydust Stuff." The antics to produce a floating scope took me back once again to the mid 50's when I was involved in modifying your N.T.S.C. system to the British 405 line system. My particular project was to produce a line timebase using only components available over here. The scan coils were at a boost voltage of approximately 800 V, and the only way to see the scan current was to float a Tektronix 524AD on a large cardboard box and hope that no one touched it. This wasn't the only hazard, E.H.T. was regulated by a shunt triode valve which produced copious amounts of X-rays, but a prominently displayed Geiger counter deterred all but the most indomitable visitors.

However, time moves on and my company now produces an "isolation amplifier" which will enable you and your friends to make measurements on floating circuits without the attendant risks to life or limb, or the purchase of yet another scope.

PETER WAUGH
Waugh Instruments Ltd.
United Kingdom

I rarely use more than 60 V, but when I do, I use an NE-2 neon lamp to remind me I'm not in 5-V land anymore. (I bet that Tek 524AD would have needed a lot of silk threads to support it.)—RAP

Dear Bob:

Just returned from Christmas holiday to find your Pease Porridge column in the Dec. 16, 1993 issue (definitely cold and more than 9 days old) discussing Reverse Pulse Charging of batteries. Christie Electric Corp. has been implementing this process in various products for more than two decades as REFLEX chargers.

The implementation of a discharge pulse interspersed between charge pulses has proven particularly effective with Nickel-Cadmium batteries (an alkaline chemistry cell). Some advantage can be gained with Lead-Acid batteries, and other chemistries such as Nickel-Metal Hydride. The optimum pulse algorithm varies depending on cell construction and chemistry.

Waaay back (late sixties, I think) there was a brief, very brief, introduction of a supposedly rechargeable manganese alkaline cell type. It disappeared quickly.

I may work up the nerve to try some "primary" alkaline cells with our equipment if I can get an adequately explosion-proof containment chamber first. I have seen even rechargeable Ni-Cd batteries explode (it's called "thermal runaway"), so the thought of pumping up a non-rechargeable cell should be carefully considered and controlled.

BILL MONAGLE
Christie Electric Corp.
Gardena, Calif.

I had no troubles with explosion or corrosion when I charged my alkalines, they just didn't hold any charge. I'm trying the Buddy L "Supercharger" next.—RAP

Dear Bob:

Now that I have a Camcorder myself, I am a bit more interested in what you have had to say about batteries and recharging. I have two questions for you on this topic. First, does anyone make NiMH batteries for camcorders yet? It seems like these would be better, and camcorder batteries are becoming more standardized. And second, why not use some sort of solar panel to charge your camcorder batteries (or replace them altogether), which could also shade your head while you hike around? Seems like that would be a good thing for Real Goods to offer.

I also enjoy your comments on Dr. Science. They don't carry him on any local stations, so I have to order the cassettes and books from Duck Breath, but that's OK. In a rather shallow attempt to avoid copyright problems, I have been working on a "Mr. Science" session for Mensa gatherings. My intention is to replace their Joke Off with my Mr. Science, since we have all heard all the jokes anyway. But unlike Dr. Science, what I am proposing is a chance for participants to tell preposterous tall tales of science outright, without the initial question. This may work at meetings of other groups as well. And it may end up being a bit like a verbal *Journal of Irreproducible Results*. I have been working on an imaginary news story about how banks are funding wormhole research, so their customers can have access to their safe deposit boxes from any branch of the bank...

It seems to me that people just don't have enough opportunities to laugh anymore. I don't know why that is, but many others agree that life has just gotten too damned serious. Within Mensa, I started a Creative Mischief SIG to help counter this. It has become quite successful, and caused many people to laugh. It also makes people read posted signs very carefully, since we tend to create hoaxes that are in the form of posted signs. Our fake ads for an imaginary "Schroedinger's Cat Sitting Service" is a hit, and almost believed by a number of people.

So, I look forward to the April 1 issue of Electronic Design and your column. Keep up the great work, and go ahead and double-clutch that VW.

MARK S. HUTCHENREUTHER
Oxnard, Calif.

I find that NiMH has only 15% more watt-hours per ounce than NiCds. But they are more dense, and pack 40% more watt-hours in a given volume. That's not a big deal when I back-pack. I don't like to depend on just solar cells on cloudy days.—RAP

More Floobydust 1993 ....

As I mentioned a couple of months ago, "floobydust" is a *recently-coined* (1976) term for "miscellaneous." Some

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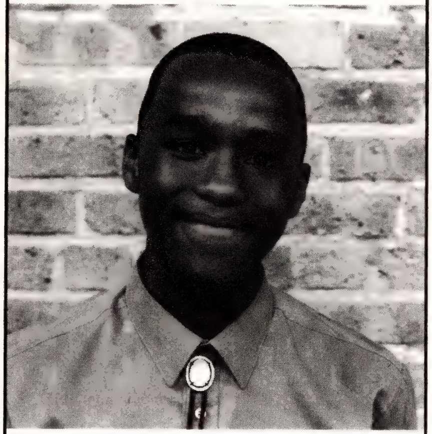

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PEASE PORRIDGE

people don't consider 1976 as recent, but I usually do.

• I got several letters from readers pointing out that Whirlpool's high-efficiency refrigerator only uses Fuzzy Logic to plan the schedule for Defrosting, avoiding the wasted energy of Defrosting when no Defrost is needed. This provides a 3% advantage over a dumb fixed-cycle defroster. That sounds pretty reasonable.

But Mr. R. Shattuck of Gillett, Pa. pointed out that it is a well-known trick among refrigerator engineers, to disconnect the Defrost timer from line power (which provides a fixed 12-hour Defrost spacing), and reconnect it to the switched power fed from the thermostat to the compressor. This way, when the door is opened a lot, or when it is a hot humid day, the Defrost cycle will run more often, and when it is a cool day, or the door is not opened much, the defrost cycle will occur less often. It is unclear how much advantage the Fuzzy Logic provides, compared to this simple but thoughtful scheme.

Note: Whirlpool is delighted to say that its prize-winning refrigerator is 29% more efficient than the 1993 Federal Efficiency Guidelines. However, it is fair to point out that this basic refrigerator was 20% more efficient than the 1993 Efficiency Guidelines, even last year, *before* they started to optimize it for the competition. So, *you* figure out, what is a Straw Man, and what is not....

• A knowledgeable spokesman for BART (Bay Area Rapid Transit) confirmed that BART trains accelerate and decelerate and run smoothly, *without* the use of Fuzzy Logic. More on this, later.

• Recently I was invited to lecture on Fuzzy Logic, with the Santa Clara Valley IEEE Measurement and Instrumentation Society. I asked the throng of 120-odd people, has anybody ever *actually* stabilized a triple inverted pendulum, using Fuzzy Logic? Or was it just *simulated*? A couple people confirmed that it was only simulated... sigh....

• As I mentioned in December—I once paid $30 for the charger station for Ray-O-Vac *Renewal* rechargeable alkaline batteries—but recently I noticed the price was now $49.95, at the same store where I bought mine....

• I finally did get some literature on the Ray-O-Vac *Renewal* rechargeable alkaline batteries. Their capacity does not shrink very rapidly with use—it is still 60% of the original capacity, after 25 cycles. However, a *Renewal* D cell is rated for just 5.5 ampere-hours when new (@ 2.7 ohms load). I was really expecting more. A conventional alkaline D cell has 14.2 ampere-hours (@ 4.7 ohms load), even though you can only use it once.

• It is true that *most* NiCd D cells, as available at popular electronics and consumer stores, pack only 1.6 ampere-hours, because most NiCd D cells are built with only a C cell inside—rather cheap and light in weight. But you can buy real D cells that pack 4+ ampere-hours, if you ask for high-capacity NiCd cells—available at Radio Shack, DigiKey, and other good electronics stores. About $18 per pair, and well worth it if you really need the energy.

• Has anybody noticed that you can no longer buy an inexpensive $10 1/4 inch electric drill? All the stores want to sell you is a fancy reversing variable-speed 3/8 inch drill, or a $50 cordless drill, or a $129 "professional grade drill." From coast to coast—what kind of conspiracy is going on? Or, can anybody tell me where I can buy a 1/4 inch drill? If they are going to become collector's items, I'll buy three. Maybe other readers would like to be able to buy one, too.

• Recently an engineer who lives in Europe pointed out that I was not very helpful if I only list 800-989-DUCK as the number for Doctor Science, because it is impossible to call an 800 number from outside the USA. So for example, if somebody wants a catalog of Doctor Science's wit and wisdom, the real telephone number, that anybody anywhere can use, is 916-265-5470. You should always list a *real* number with the 800 number.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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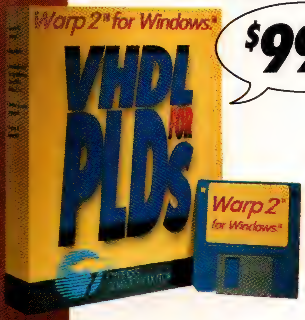

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A SPECIAL EDITORIAL FEATURE

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ELECTRONIC DESIGN

SMT Interconnections Evolve Beyond Solder

As SMT connectors mature, a bevy of alternatives come to light.

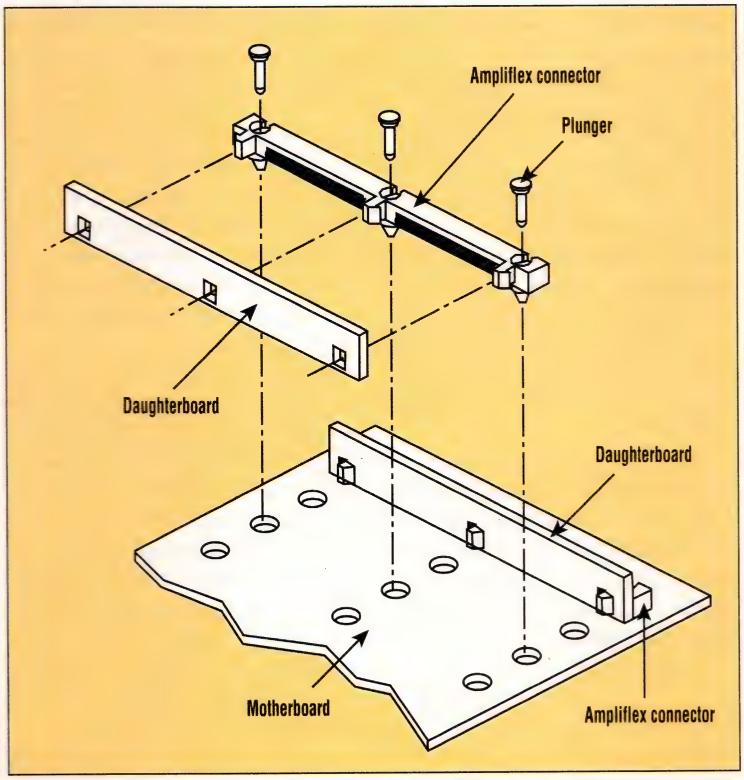
BY DICK GRANITZ

AMP Inc., P.O. Box 3608, Harrisburg, PA 17105-3608; (717) 986-7119.

Surface-mount technology (SMT) continues to play a crucial supporting role in the OEM electronics industry's ongoing trend toward smaller, faster, and less costly end products. The reasons: SMT offers advantages in packaging density, manufacturing efficiencies, and reliability.

But taking full advantage of SMT's space, weight, and cost savings involves simplifying assembly procedures so that there's just one processing method for soldering. Connectors were among the last components to be available in surface-mount versions. Early concerns involved long-term reliability of the relatively large connectors. The chance of solder-joint failure from differences in thermal expansion, board warpage, or rough handling during mating/unmating increases with a component's size. Such concerns have been answered by addressing the compliancy, hold-down, and thermal properties of the application and connector.

A key element of SMT is the ability to assemble and reflow-solder a board on a single line without such secondary processing as hand assembly of components or wave soldering. As a result, compatibility with surface-mount processing techniques is often as important as a true surface-mount connector.



1. The basic elastomeric strip can be easily adapted to many connector styles. A variety of low-cost housing configurations permit the strip to be used in numerous applications. Here, a mother-to-daughterboard application is shown.

Large connectors—those with centerlines of 0.100 inches—have been redesigned or converted for SMT, while remaining through-hole components. Through-hole components have been redesigned by changing housing materials to ones that can withstand reflow soldering. This permits simultaneous reflow of all components including connectors.

Such conversions typically mean redesigning the connector with tighter dimensional tolerances and materials that withstand both the heat of reflow soldering and the harshness of cleaning solvents. Such connectors must also include tolerancing and packaging for use with pick-and-place equipment, and a board-retention feature to hold the connector for soldering.

Nearly all new through-hole connectors are being designed for SMT process compatibility. Others, notably subminiature-D, circular DIN, modular jacks, and SIMM connectors, are offered in true SMT versions.

Fine-pitch connectors and IC sockets with contact centerlines of 0.050 inches or less are better candidates for surface mounting because of their smaller size. Thermal-mismatch problems have proven to be less significant than originally expected. What's more, as connector densities increase, surface mounting becomes mandatory. Wave soldering grows more difficult below centerlines of 2 mm and impractical below 1 mm.

SMT sockets and connectors for both board-to-board and wire-to-board applications are now widely available. "True" surface-mount connectors are fully compatible with today's SMT assembly and processing requirements. Such connectors can be mounted on standard EIA 481 tape and handled for standard pick-and-place equipment. Matrix trays and gravity-fed tubes form alternative feed systems, but with less compatibility when using pick-and-place equipment. While many users are comfortable with tubes, the use of trays is declining except where made necessary by large, odd-shaped devices or robotic processing.

Though pick-and-place compatibility also requires a flat surface for vacuum pickup, the open shape of connectors presents difficulty in providing a surface. As a result, some vendors use a peel-off plastic insert for vacuum pickup.

To facilitate visual solder-joint inspection, most surface-mount connectors have two rows and gull-wing leads. The gull-wing design offers the best solder joint strength, compliancy, and ease of inspection and repair, but at the expense of space conservation. Butt joints have been declining in popularity, while J leads remain a favorite with IC sockets. Emerging density requirements may reduce the demand for visual inspection because of the limits it places on connector and lead geometry.

Connector technology has always been driven by the technology behind the devices being linked. While small contacts offer a short propagation delay to high-speed signals, impedance matching may be necessary in connectors intended for high-speed operation. Greater attention will be paid in future connectors when it comes to meeting the transmission-line properties of the connector and maximizing the number of signal lines per unit area.

Traditionally, surface-mount connectors and sockets have accommodated peripheral arrays, where the contacts run around the edge of the device. Two-row connectors and four-sided PQFPs are examples of peripheral arrays. One advantage of peripheral arrays is that solder joints can be easily inspected visually and soldering processes are straightforward and well understood. Area arrays—four-row connectors and pin- and land-grid array ICs—aren't so easily accommodated. Many alternatives to solder have been designed to handle area-array applications.

Green also is in. Just as environmental awareness has led the industry to eliminate CFC-based cleaning in favor of aqueous cleaning, there's a desire to eliminate or reduce the use of lead, including that which is in solders. Alternative approaches like compressive connectors eliminate solder, while techniques such as solder balls tend to be "clean" approaches that yield little residual solder.

Compressive techniques for achieving a reliable interconnection between connector and board offer an alternative to solder. Such techniques eliminate solder and allow high-density interconnects adaptable to many packaging needs. Although soldering remains the preferred solution for many packaging and manufacturing engineers—solder, after all, has a long, proven track record—compressive techniques allow packaging solutions that are impractical with solder. The three most popular compressive techniques are metal contacts, elastomeric, and flexible etched circuits. Each share the need for a secondary mechanical fastening and backup to the board by screws, latches, or other means. Here's some information specific to each type:

SMT-process compatibility is often as important as having a true SMT connector.

Metal-contact compressive connectors: Compressive techniques are popular where soldering is impractical. Land grid array (LGAs), which use an array of pads on the bottom of the package, aren't intended to be soldered. LGA sockets use an array of contacts to form a spring-loaded gas-tight connection between the device and board. A precision housing holds the contacts and LGA in alignment, while an underboard alignment and backup plate provides the clamping retention to keep the contacts pressed tight against the board. Fully compressed, the contact height is a scant 0.009 in., permitting a very low socket profile. Obviously, the low contact height also provides a short electrical path for high-speed signals with a propagation delay of 8 ps.

Compressive metal contacts also have been used to interconnect fine-pitch multichip modules containing several hundred I/O connections. Such connectors permit contact spacing as tight as 0.010 in. A short electrical path aids high-speed operation with minimal signal distortion or delay.

In high pin-count applications, forces can become quite high, requiring upwards of 100 lbs. to maintain enough normal force to achieve a reliable, gas-tight joint. For example, the normal force on a joint is at least 100 g/contact for a tin-plated connection and 50 g/contact for contacts plated with gold or other precious metals. Careful contact design can lower the mating forces for such contacts.

Elastomeric connectors: Connectors based on a resilient rubber core offer a low-cost alternative to solder when connecting two planar surfaces, including ceramic substrates, flex cables, pc boards, and displays. While

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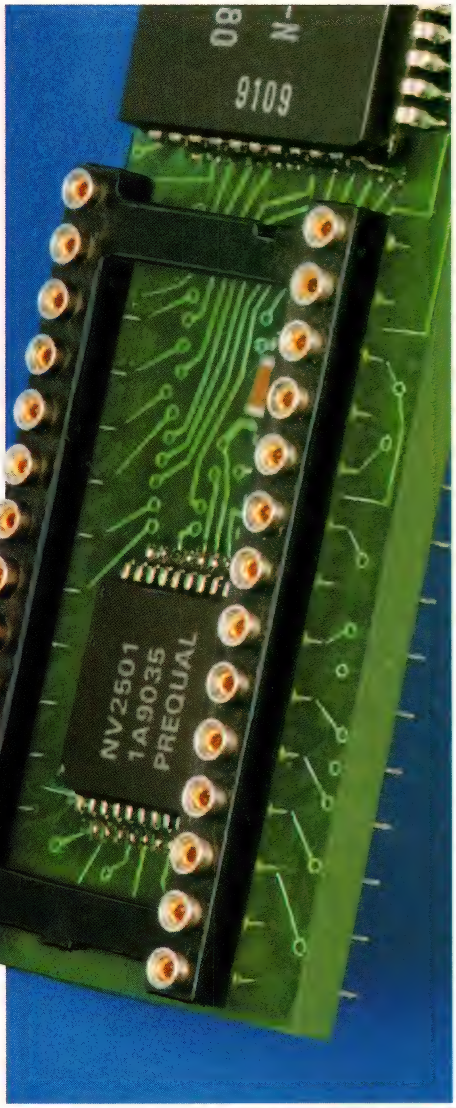

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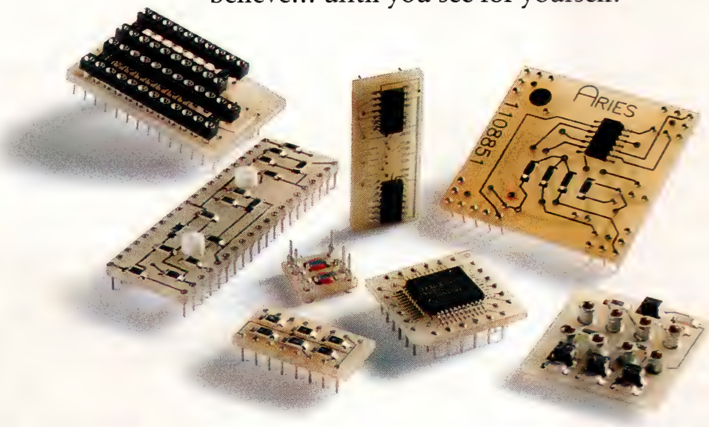

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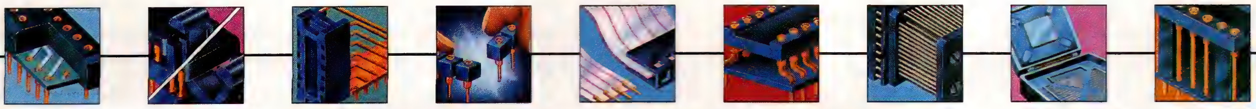

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elastomeric technology is not new, its ability to create dense, high-pin-count interconnections at relatively low cost is bringing about a renaissance.

Conductors can be formed on the core by a number of methods. One approach is to cover the core with a thin, flexible polyimide film and then deposit parallel lines of gold-plated etched copper over the film. A typical film consists of 0.003-in. copper lines on 0.007-in. centers. This provides redundant contact—more than one copper line on each board pad—for board pads as small as 0.015 in. wide on 0.025-in. centers. The gold-plated copper conductors provide a contact resistance under 100 mΩ and a current rating of 500 mA on a 0.015-in. pad.

Another method puts conductive additives directly into the elastomer. Additives include silver ink, carbon particles, and carbon fibers. One low-cost approach is conductive carbon, which uses non-woven carbon particles impregnated in silicone rubber. An insulating layer of pure silicone rubber separates each conductive layer.

In application, the two planar surfaces to be joined form a gas-tight interface with the elastomeric connector. The elastomer is highly tolerant of uneven surfaces and resists compression set so that adequate contact pressure is maintained.

The basic elastomeric strip can be easily adapted to a number of connector styles. Various low-cost housing configurations permit the strip to be used in many different applications, including connecting grid-array sockets, multichip modules, flex-film-to-pc-board, board stacking, and more *(Fig. 1)*.

The short interconnection path and outstanding electrical properties of elastomeric connectors makes them ideal for high-speed signal propagation. For very high speeds over long paths, controlled-impedance board patterns are available to provide minimal signal reflections and distortions. Because the elastomeric member can have a free-height diameter as small as 0.040 in., it presents a low propagation delay. Low-resistance designs offer a resistance of 20 mΩ, inductance of 1 nH, and capacitance of 0.2 pF. Propagation delay is 12 ps.

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2. Recent advances in application technology have made solder-ball technology practical and cost-effective for a wide range of users. In this demonstration, 60-μm balls are placed on 200-μm centers.

Flexible etched circuitry: Connectors using flexible etched circuits (FECs) in place of traditional stamped electrical contacts meet the speed and density requirements of future systems. One system uses FECs wrapped around a rectangular housing assembly. Channels in the housing hold canted-coil springs. The springs provide a near-constant normal force over a wide range of deflections, which makes the connector easy to use in tolerance-sensitive applications. The housing, which is plastic or aluminum, surrounds a solid metal-core structural member that gives the system a rigid structure. Finally, plastic or metal end caps provide a means of securing the connector to the board. The system is solderless and uses mechanical fastening to achieve a compression connection. The new connector borrows from materials-processing technologies used to make the printed-circuit boards to which they connect.

Flexible etched circuits are essentially flexible printed-circuit boards. They're made from alternating layers of conductive materials, such as rolled, annealed, or electrodeposited copper, and flexible dielectrics like polyester or polyimide. Conductive layers are patterned, typically using photolithographic and liquid-etching processes, to create electrical contact areas and conductive pathways. Conductive layers can be electrically interconnected as required to route signals and maintain geometric relationships among signals to achieve desired electrical performance.

By combining the small features of FECs with the concept of an area array, it's possible to achieve practical densities of 200 signal lines per linear inch. A FEC can be routinely produced with a 0.004-in.-wide conductor on 0.008-in. spacing. In principle, this yields an interconnection density of 125 lines per inch. Such a connector, however, would be impractical to connect (permanently, or separably) to its mating printed-circuit boards. The solution is to use a multi-row area array of electrical connections rather than a single row. By using this approach, high densities can be achieved without the need to cram tiny contacts together as is necessary in a simple linear single row. A tightly spaced single row presents tolerance difficulties because of the fine pitches involved.

Many of the emerging trends in surface-mount connectors involve the evolution of smaller, denser devices. Spacing for centerlines is reaching 0.025 in. and tighter, with 1-mm centerlines available but not yet widespread. As the demand for smaller, faster portable PCs and personal communicators grows, new connector families will meet these needs. But even as

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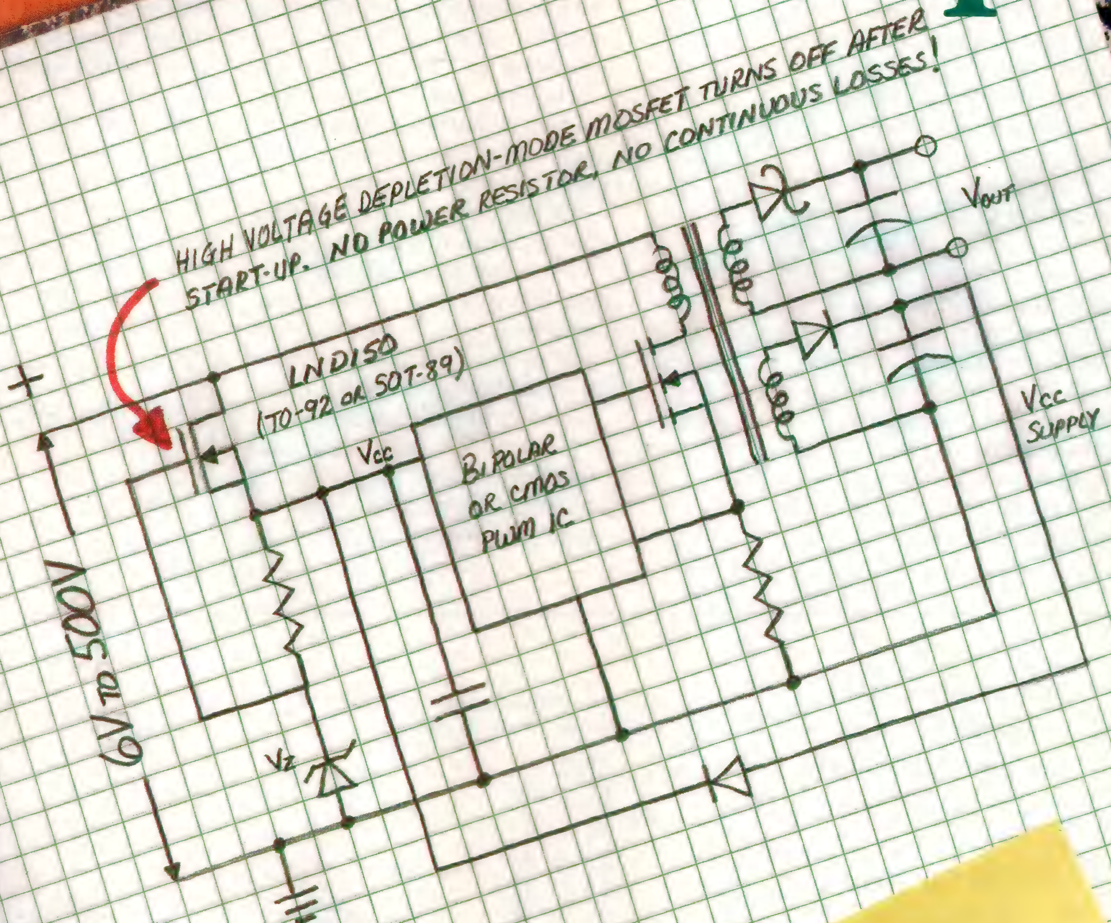
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connectors become available, other techniques will offer solutions to packaging problems not easily addressed by existing connectors. Two main techniques are solder balls and conductive adhesives.

Despite the advantages of compressive techniques in interconnecting area arrays, many users are more comfortable using solder. Solder balls may provide the answer. Though solder-ball technology isn't new, recent advances in application technology have made it practical and cost-effective for a wide range of users. Solder-jet technology, somewhat akin to inkjet-printer technology, can precisely place 100-μm balls on 200-μm spacings *(Fig. 2)*. Conventional X-Y positioning systems possess the accuracy to position the board for solder placement. The highly controlled process has quality built in, eliminating the need for inspection. Soldering area arrays requires such an approach to quality. Simply put, defect prevention is key to reliable, cost-effective assembly.

Solder-jet balls will become important as spacing requirements pass 0.015 in. Board densities are already reaching the point to where solder screening becomes difficult and first-pass yields are low. An additional benefit is that solder-jet technology wastes no solder and has no leftover lead to discard.

Solder balls still require careful thermal matching. Device sockets can act as a buffer offering compliancy to absorb mismatched CTE between board and device. Indeed, the solder ball can be applied either to the socket or to the board.

Conductive adhesives have found electronic application in consumer devices for years. To many, however, questions of long-term reliability have prevented wider use in commercial and industrial applications. In the absence of long-term environmental testing, users are still reluctant to commit their systems to adhesives. Nonetheless, adhesives remain attractive if their long-term reliability over a range of application environments can be shown.

Dick Granitz, associate director of interconnection research, manages special programs for AMP Interconnection Systems. His 25-year career with AMP spans product management, development engineering, and systems packaging.

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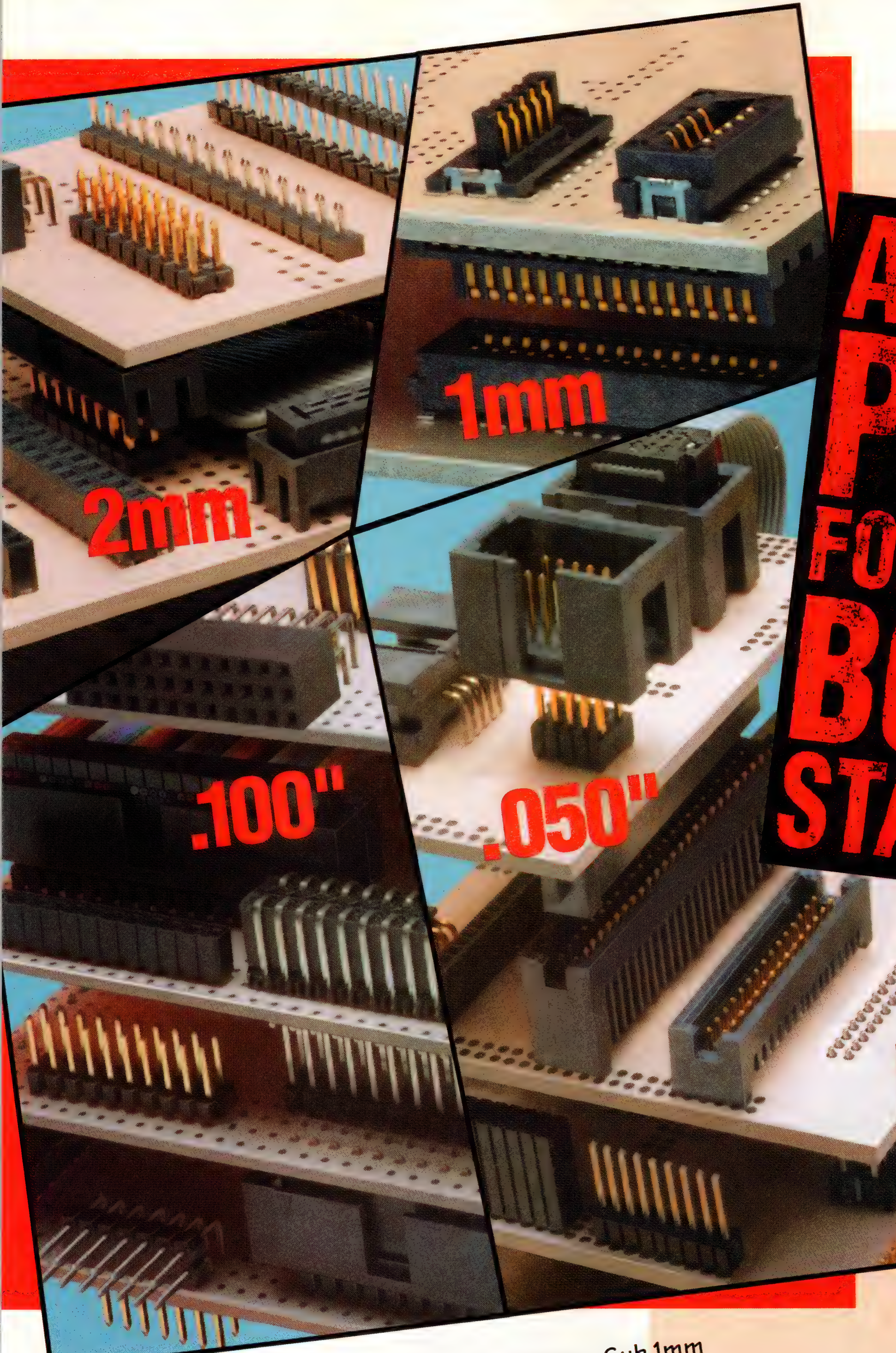

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(GP) (CN) (VR) (PT) (CM)
CIRCLE 814

Augat Inc.
Interconnect Products Div.
452 John Dietsch Blvd.
North Attleboro, MA 02760
(508) 699-7646
(DI) (FC) (CE) (ZI) (DP) (PG)
CIRCLE 815

BICC-Vero Electronics Inc.
1000 Sherman Ave.
Hamden, CT 06514
(203) 288-8001
(DI) (BP) (VB) (MB) (IB) (BU)
(GP) (CN) (IN) (VR) (WT) (PT)
(EM) (CM) (ER)
CIRCLE 816

Belden Wire & Cable Co.
P.O. Box 1980
Richmond, IN 47375
(317) 983-5200
(CO) (FL) (TW) (SH) (PW)
CIRCLE 817

Berg Electronics Inc.
150 Corporate Dr., Suite 201
Camp Hill, PA 17011
(800) 237-2374
(CX) (DS) (DI) (FC) (CE) (ID)
(ZI) (SM) (CC) (CD) (HC) (RP)
(FO) (FL) (SH) (HN)
CIRCLE 818

Bravo Communications Inc.
1310 Tully Rd., Suite 107
San Jose, CA 95122
(408) 297-8700
(AU) (CX) (DS) (CO) (FL)
(TW) (SH) (ES) (MG) (ER)
CIRCLE 819

Bud Industries Inc.
4605 E. 355th St.
Willoughby, OH 44094
(216) 946-3200
(GP) (CN) (IN) (VR) (PT)
(EM) (CM)
CIRCLE 820

CTI Technologies Inc.
7855 E. Evans Rd., Suite A
Scottsdale, AZ 85260
(602) 998-1484
(CC) (BI)
CIRCLE 821

CTS Connector Products
9210 Science Center Dr.
New Hope, MN 55344
(612) 533-3533
(SM) (MD) (ML) (BP) (VB)
(SB) (MB) (GB)
CIRCLE 822

CW Industries
130 James Way
Southampton, PA 18966
(215) 355-7080
(DS) (DI) (FC) (CE) (ID)
(SM) (CD) (MD) (RP)
CIRCLE 823

Cambion Interconnection Products Ltd.
P.O. Box 402
Topsfield, MA 01983
(800) 947-1256
(ID) (SM) (DP) (PG)
(CD) (MD)
CIRCLE 824

Chomerics Inc.
77 Dragon Ct.
Woburn, MA 01888
(617) 935-4850
(ER) (GK) (FR) (SE) (TB)
(RC) (VE)
CIRCLE 825

Cole-Flex Corp.
91 Cabot St.
West Babylon, NY 11704
(516) 249-6150
(TB)
CIRCLE 826

Comm Con Connectors Inc.
1848 Evergreen St.
Durante, CA 91010
(818) 301-4200
(FC) (ID) (ZI) (SM) (DP) (CD)
CIRCLE 827

Components Corp.
6 Kinsey Pl.
Denville, NJ 07834
(201) 627-0290
(CE) (SM) (CC)
CIRCLE 828

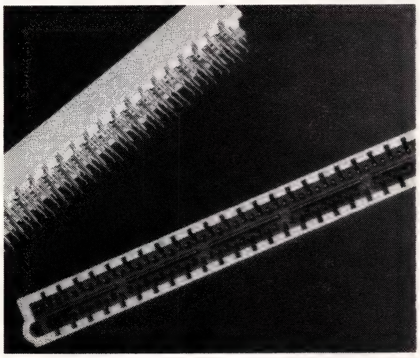
Dawn VME Products Inc.
47073 Warm Springs Blvd.
Fremont, CA 94539
(800) 258-DAWN
(BP) (VB) (GB) (GP) (BM)
(VR) (CM)
CIRCLE 829

(see p. 146 for key)

(continued on p. 140)

▼ CONTROLLED-Z CONNECTOR PROTECTS ITS CONTACTS

Enhancements to the Micro-Strip connector family of high-density, controlled-impedance board-to-board and cable-to board connectors have lowered the receptacles' contact insertion force and improved contact protection. The connectors contain 40 high-speed signal lines and their associated grounds per linear inch. Signal transmission is performed with minimal distortion from crosstalk or ground bounce. Insertion forces have been reduced by 25%, and the units' housings feature a funneled lead-in to protect against stubbing or other damage during mating. Pricing ranges from $0.15 to $0.25 per line depending on quantity. Delivery is in eight weeks.



AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
▶CIRCLE 630

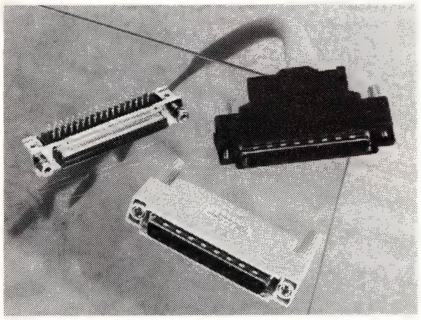
▼ TEST/BURN-IN SOCKETS CUT BGA TOOLING COSTS

A family of test and burn-in sockets dramatically reduces tooling costs and turn-around time for ICs in ball-grid-array packages, such as Motorola's OMPAC, and land-grid-array packages. The sockets' modular design eliminates the need for expensive dedicated tooling for each package variant. The basic socket sizes provide for a wide range of device sizes. The first socket size accepts packages up to 23 mm^2 in either 60-mil or 1.5-mm pitches. The second size accepts packages up to 38 mm^2 at 50-mil or 1.5-mm pitches. Call for pricing and delivery.

3M Electronic Products Div.
6801 River Place Blvd.
Austin, TX 78726-4599
(800) 328-0411
▶CIRCLE 631

▼ SCSI-3 CONNECTOR HELPS SPEED UP DATA

An ANSI-approved SCSI-3 connector series provides a standard external interface between PCs and workstations and external storage devices using an expanded transfer-bit width to accommodate faster processing speeds. The FCN230-R Series includes a 68-position, right-angle, board-mounted socket and an IDC cable-mount plug with 0.050-in. contacts and a pin-and-tuning-fork connection design. A backshell and a connector with a built-in differential terminating resistor are also included in the series. Pricing for a socket and cable-mount plug with backshell is $11.97 in lots of 5000. Delivery is from stock.



Fujitsu Microelectronics Inc.
Electronic Components Div.
3545 N. First St.
San Jose, CA 95134
(800) 642-7616
▶ CIRCLE 632

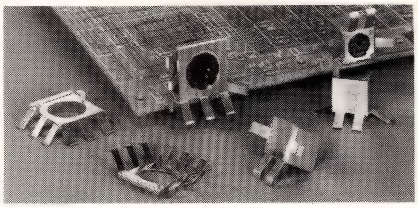
▼ SMT PLCC SOCKETS ACCEPT UP TO 84 LEADS

Available in 20 through 84 pins, the 709-2001 Series surface-mounted PLCC sockets accept industry-standard J-leaded devices. The plastic carriers feature a skeleton base that permits visual inspection of the soldered joints before assembly of the device. This removes the possibility of poor soldering causing equipment to fail. Other features include board stand-offs to facilitate board cleaning and locating pegs for socket orientation. Call for pricing.

Cambion
P.O. Box 402
Topsfield, MA 011983
(800) 947-1256
▶ CIRCLE 633

▼ DIN-PLUG GASKETS MAKE GROUND TO CHASSIS

A series of gaskets for grounding DIN plugs to computer chassis can also be used for grounding circuit boards, keyboards, and audio equipment. Made of beryllium copper, the gaskets exhibit excellent conductivity and attenuation characteristics. Their universal configuration fits most DIN plugs, and a slide-on design makes assembly easy. A wide variety of plating finishes is offered, as are gaskets with or without formed bends to accommodate different-sized connectors. Call for pricing and delivery.



Instrument Specialties Co. Inc.
P.O. Box A
Delaware Water Gap, PA 18327
(717) 424-8510
▶ CIRCLE 634

CONNECTOR AND PACKAGING MANUFACTURERS

Deutsch
Commercial Products Div.
700 S. Hathaway
Banning, CA 92220
(909) 849-4568
(SM) (CD) (MD) (HV) (HC) (HN)
CIRCLE 830

Dimensional Circuits Corp.
9400-K Activity Rd., #K
San Diego, CA 92126
(619) 549-4290
(PG) (CD)
CIRCLE 831

ERNI Components Inc.
520 Southlake Blvd.
Richmond, VA 23233
(804) 794-6367
(RF) (CX) (DS) (DI) (CE) (ID) (SM) (MD) (HV) (HC) (FO) (CM)
CIRCLE 832

Eby Co.
4300 North H St.
Philadelphia, PA 19124
(215) 537-4700
(AU) (CE) (CD) (MD) (HV) (HC) (FX) (BP) (HN)
CIRCLE 833

Elco U.S.A.
Huntington Industrial Park
Huntington, PA 16652
(814) 653-0700
(DI) (FC) (CE) (ID) (ZI) (SM) (CD) (MD) (RP)
CIRCLE 834

Elcon Products Int'l. Co.
P.O. Box 1885
Fremont, CA 94538
(510) 490-4200
(CD) (MD) (HC) (RP)
CIRCLE 835

Eldre Corp.
1500 Jefferson Rd.
Rochester, NY 14623
(716) 427-7280
(BB)
CIRCLE 836

Electrical Insulation Suppliers
300 N. Mannheim Rd.
Hillside, IL 60162
(708) 547-5400
(SS) (DD) (ML) (PC) (CO) (FL) (TW) (SH) (WV) (PW) (MN) (HK) (HN) (CA) (BB) (ES) (MG) (ER) (GK) (FR) (SE) (TB) (RC) (VE) (WN)
CIRCLE 837

Electronic Solutions
6790 Flanders Dr.
San Diego, CA 92121
(619) 452-9333
(WR) (BP) (VB) (MB) (BU) (GP) (BM) (VR) (EM) (CM)
CIRCLE 838

Elform Inc.
P.O. Box 7362
Reno, NV 89510
(702) 829-1905
(EL)
CIRCLE 839

Elma Electronic Inc.
44350 S. Grimmer Blvd.
Fremont, CA 94538
(510) 656-3400
(DI) (ML) (WR) (BP) (VB) (MB) (IB) (BU) (SH) (HN) (BB) (GP) (IN) (VR) (WT) (PT) (EM) (MI) (CM) (ER) (GK)
CIRCLE 840

Elmec Manufacturing
4127 Avenida De La Plata
Oceanside, CA 92056
(619) 631-0202
(FC) (DP) (CD) (FX) (FL) (SH) (HN)
CIRCLE 841

Emcor Products/Crenlo Inc.
1600 N.W. Fourth Ave.
Rochester, MN 55901
(507) 289-3371
(GP) (CN) (IN) (VR) (WT) (EM) (MI) (CM) (ER)
CIRCLE 842

Emulation Technology Inc.
2344 Walsh Ave., Bldg. F
Santa Clara, CA 95054
(408) 982-0660
(ZI) (SM) (CC) (DP) (PG) (CD) (BI)
CIRCLE 843

Equipto Electronics Corp.
351 Woodlawn Ave.
Aurora, IL 60506-9988
(708) 897-4691
(GP) (BM) (CN) (IN) (VR) (PT) (EM) (MI) (CM)
CIRCLE 844

Feller U. S. Corp.
72 Veronica Ave., Unit #4
Somerset, NJ 08873
(908) 247-7333
(SH) (PW) (HN)
CIRCLE 845

Fujitsu Microelectronics Inc.
Electronic Component Div.
3545 N. First St.
San Jose, CA 95134-1804
(800) 642-7616
(DS) (FC) (CE) (ID) (SM) (DP) (CD)
CIRCLE 846

G & H Technology Inc.
750 W. Ventura Blvd.
Camarillo, CA 93010
(805) 484-0543
(CD) (MD) (FO) (ES) (ER)
CIRCLE 847

Garrett Electronics Corp.
149 Geary Ave.
New Cumberland, PA 17070
(717) 774-7923
(DS) (FC) (CE) (ID) (CD) (FL) (TW) (SH) (PW) (HK) (HN)
CIRCLE 848

Garry Electronics
WPI Inc.
23 Front St.
Salem, NJ 08079-1047
(609) 935-7601
(DS) (ZI) (PG)
CIRCLE 849

Graphic Research Inc.
9334 Mason Ave.
Chatsworth, CA 91311
(818) 886-7340
(SS) (DD) (ML) (FX) (BP) (PC)
CIRCLE 850

Haewa Corp.
4357-B Park Dr.
Norcross, GA 30093
(404) 921-3272
(GP) (BM) (CN) (IN) (VR) (WT) (CM)
CIRCLE 851

Handy & Harman Tube Co. Inc.
701 E. Township Line Rd.
Norristown, PA 14403-4629
(215) 539-3900
(TB)
CIRCLE 852

Harting Elektronik Inc.
2155 Stonington Ave., #212
Hoffman Estates, IL 60195
(708) 519-7700
(CX) (DS) (DI) (FC) (ID) (HV) (HC) (RP) (FO)
CIRCLE 853

Hirose Electric (U.S.A.) Inc.
2688 Westhills Ct.
Simi Valley, CA 93065-6235
(805) 522-7958
(AU) (RF) (CX) (DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CC) (DP) (PG) (CD) (MD) (HV) (HC) (RP) (FO) (CO) (FL) (MG) (ER)
CIRCLE 854

(see p. 146 for key)
(continued on p. 142)

YOU SHOULDN'T HAVE.
YOU SHOULDN'T HAVE.

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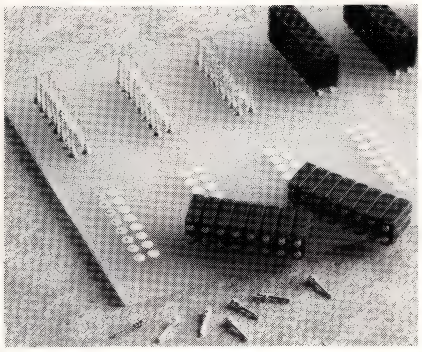
A public service of this magazine

▼ 2-MM PIN HEADERS IN DISPOSABLE CARRIERS



Easy carrier removability is the key to the 2-mm pin-header carrier system. The system features a specially designed pin that's loaded into the carrier. The pin has a round base with a channel encircling its midpoint, which optimizes the strength of the solder joint. Soldered to 1.75-mm-diameter round pads on a 2-mm pitch, the footprint of the dual-row version measures just 3.5 mm wide. After soldering, the carrier is removed, leaving the pins soldered directly to the pc board without any insulator. As a result, a shunt or female header mated to the pins will have a lower profile. Three above-board heights of 2.4, 3.5, and 5 mm are available. Pricing in lots of 10,000 for a 2-by-4-position, 2.4-mm-tall carrier with 15-μin. gold-plated pins is $0.15 each.

McKenzie Technology
910 Page Ave.
Fremont, CA 94538
(510) 651-2700
▶CIRCLE 635

▼ LOCKING POWER PLUG OFFERS SECURITY

Two versions of a two-conductor, miniature locking power plug both feature a knurled lock ring that threads onto the mating jack to hold the connection securely. Version 760K has a hollow, 0.325-in.-deep center pin with a 0.100-in.-diameter center hole. It mates with two-conductor power jacks such as the Switchcraft 712A. Version S760K has a 0.08-in.-diameter hole and mates with power jack 722A. The plugs are well suited for various applications including medical, instrumentation, audio, and computer systems. Pricing is $3.50 in OEM lots with delivery in six to eight weeks.

Switchcraft Inc.
5555 N. Elston Ave.
Chicago, IL 60630
(312) 792-2700
▶CIRCLE 636

▼ RF-COAX CONNECTOR SOLVES MATING PROBLEMS

A wide variety of standard and custom-made RF-coaxial connector adapters solves mating problems between different types of plugs, jacks, and receptacles. The adapters come in over 100 standard designs including N-to-BNC, N-to-LC, N-to-SC, BNC-to-HN, N-to-C, and many more. Bodies are made from brass, bronze alloys, beryllium copper, and other materials with insulations, gaskets, and finishes that depend on the desired performance characteristics.

Tru-Connector Corp.
245 Lynnfield St.
Peabody, MA 01960
(508) 532-0775
▶CIRCLE 637

CONNECTOR AND PACKAGING MANUFACTURERS

Hybricon Corp.
12 Willow Rd.
Ayer, MA 01432
(508) 772-5422
(SS) (DD) (ML) (WR) (BP) (VB) (MB) (BU) (GB) (GP) (BM) (VR) (PT) (EM) (CM)
CIRCLE 855

Hypertronics Corp.
16 Brent Dr.
Hudson, MA 01749
(800) 225-9228
(CE) (ZI) (CD) (MD) (BI) (HV) (HC) (RP)
CIRCLE 856

ITT Cannon
Commercial/Industrial
1851 E. Deere Ave.
Santa Ana, CA 92705
(714) 261-5300
(AU) (DS) (DI) (ZI) (SM) (CD) (RP) (FO) (ER)
CIRCLE 857

ITT Pomona Electronics
1500 E. 9th St.
Pomona, CA 91766
(714) 623-3463
(AU) (RF) (CX) (SM) (DP) (PG) (CD) (GP) (PT)
CIRCLE 858

Industrial Custom Products Ltd.
5200 Quincy Ave.
Mounds View, MN 55112
(612) 785-2266
(CC) (ES) (ER) (GK)
CIRCLE 859

Instrument Specialties Co. Inc.
P.O. Box A
Delaware Water Gap, PA 18327
(717) 424-8510
(RF) (DS) (DI) (EL) (CD) (ES) (ER) (GK) (SE) (TB) (VE)
CIRCLE 860

Interlogic Industries
85 Marcus Dr.
Melville, NY 11747
(516) 420-8111
(ML) (WR) (BP) (VB) (MB) (IB) (IN)
CIRCLE 861

Interplex Industries
Teka Interconnection Systems
45 Salem St.
Providence, RI 02907
(401) 785-4110
(DI) (CE) (SM) (CD)
CIRCLE 862

Ironwood Electronics Inc.
P.O. Box 21-151
St. Paul, MN 55121
(612) 431-7025
(ZI) (SM) (DP) (PG) (CD) (BI) (WR) (PC)
CIRCLE 863

J.S.T. Corp.
1200 Business Ctr. Dr., #400
Mt. Prospect, IL 60056
(708) 803-3300
(DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CD) (HV) (HC)
CIRCLE 864

JAE Electronics Inc.
142 Technology Dr., Bldg. 100
Irvine, CA 92718
(714) 523-2600
(DS) (FC) (CE) (ID) (ZI) (SM)
CIRCLE 865

Kycon Cable & Connector Inc.
1810 Little Orchard St.
San Jose, CA 95125
(408) 295-1110
(AU) (CX) (DS) (DI) (FC) (CE) (ID) (ZI) (SM) (CC) (PG) (CO) (TW) (SH) (PW) (ER)
CIRCLE 866

L-Com Inc.
1755 Osgood St.
North Andover, MA 01845
(508) 682-6936
(RF) (CX) (DS) (CO) (TW) (SH)
CIRCLE 867

LEMO USA Inc.
335 Tesconi Cir.
Santa Rosa, CA 95401
(800) 444-5366
(AU) (RF) (CX) (SM) (CD) (HV) (HC) (FO)
CIRCLE 868

LZR Electronics Inc.
8051 Cessna Ave.
Gaithersburg, MD 20879
(301) 921-4600
(AU) (CX) (DS) (DI) (FC) (CD) (RP) (FL) (PW) (ER)
CIRCLE 869

Lansing Instrument Corp.
P.O. Box 730, 750 Willow Ave.
Ithaca, NY 14851-0730
(607) 272-3265
(GP) (BM) (IN) (CM)
CIRCLE 870

Lumberg Inc.
11351 Business Center Dr.
Richmond, VA 23236
(804) 379-2041, ext. 301
(AU) (DI) (FC) (ID) (SM) (PW)
CIRCLE 871

Lutze Inc.
1911-A Associates Lane
Charlotte, NC 28217
(704) 357-8835
(FL) (SH) (PW)
CIRCLE 872

Markel Corp.
P.O. Box 752
Norristown, PA 19404
(215) 272-8960
(SH) (HK) (CA) (TB)
CIRCLE 873

McKenzie Technology
910 Page Ave.
Fremont, CA 94538
(510) 651-2700
(ZI) (SM) (CC) (DP) (PG) (CD)
CIRCLE 874

Meritec
Div. of Associated Enterprises
1359 W. Jackson St.
P.O. Box 8003
Painesville, OH 44077
(216) 354-3148
(CX) (FC) (CE) (SM) (PG) (CD) (RP) (CO) (FL) (TW) (SH) (WV)
CIRCLE 875

Methode Electronics Inc.
Corporate Sls./Mktg.
7444 W. Wilson Ave.
Chicago, IL 60656
(708) 867-9600
(DI) (CE) (ID) (ZI) (SM) (CC) (CD) (FO) (SS) (DD) (ML) (FX) (PC) (HN) (BB)
CIRCLE 876

Micro Plastics Inc.
Connector Div.
9180 Gazette Ave.
Chatsworth, CA 91311
(818) 882-0244
(CE)
CIRCLE 877

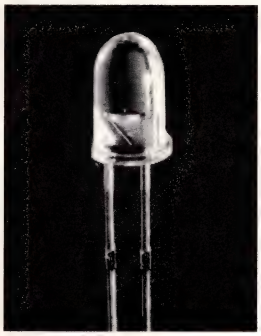
Mill-Max Mfg. Corp.
190 Pine Hollow Rd.
Oyster Bay, NY 11771
(516) 922-6000
(ZI) (SM) (CC) (DP) (PG) (CD)
CIRCLE 878

Minco Products Inc.
7300 Commerce Ln.
Minneapolis, MN 55432
(612) 571-3121
(FX)
CIRCLE 879

(see p. 146 for key)
(continued on p. 144)

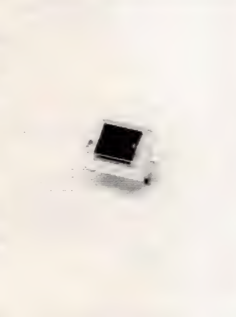
OPTIMIZED OPTICS

The VTE1295 high output IR Emitting Diode (IRED) incorporates an aspheric lens to optimize the amount of power focused into its output beam. This 5 mm diameter plastic package contains a880 nm high efficiency IRED chip. Typical power output at 100 mA drive is 20 mW. Typical total half power beam angle is 16 degrees. The VTE is U.L. Component Recognized. Applications include smoke detectors, remote controls, and security systems. CONTACT: EG&G Optoelectronics, Vactec Division, 10900 Page Ave.,St. Louis, MO 63132, Phone: (314) 423-4900, FAX: (314) 423-3956



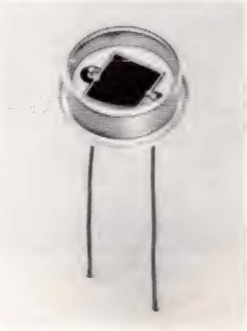
MAXIMUM PERFORMANCE IN MINIMUM SPACE

These Mini-DIP plastic packages house silicon photodiodes with an active area of 6.8 square millimeters.They offer maximum output in minimum board space. The VTD34 is molded inwater clear plastic and the VTD34F is molded in IR transmitting/visible blocking plastic. Arrays can be formed by suitably mounting individual units. Delivering low dark currents under bias and fast response speed,these units are used as light detectors in scanners, security equipment,and cameras. CONTACT: EG&GOptoelectronics, Vactec Division,1900 Page Ave., St. Louis, MO 63132Phone: (314)423-4900, FAX:(314)423-3956



LIGHT DETECTOR MIMICS HUMAN EYE RESPONSE

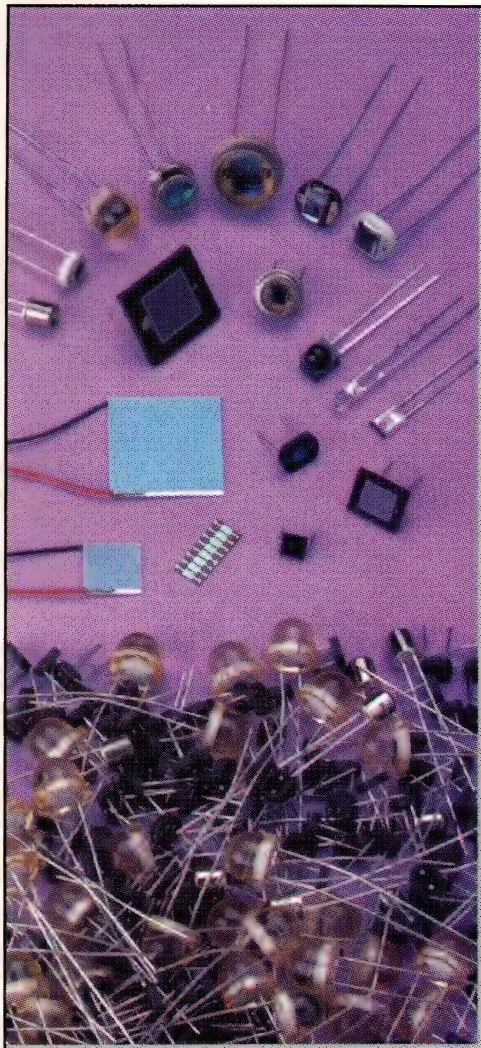
The VTB6061CIE filtered photodiode has a spectral response which closely resembles the human eye.This makes it an ideal choice for photometric applications such as precision lighting controls, spectro photometers, photographic, and video instrumentation. Photometric sensitivity is typically120 nA/fc (11 nA/lux). Features include very high shunt impedance which supports low light level measurements, low noise, and low capacitance. CONTACT: EG&G Optoelectronics, Vactec Division, 10900 Page Ave.,St. Louis, M 63132. Phone: (314) 423-4900 FAX: (314) 423-3956.



PHOTODIODE DATABOOK

The Vactec Division of EG&G Optoelectronics has published a 128 page optoelectronics databook featuring silicon photodiodes. This designer'sreference manual is a comprehensive guide to understanding, selecting,and configuring a myriad of photodetector circuits utilizing over100 standard photodiode types, including detector arrays. Clear and concise technical notes address topics such as:What is a photodiode ? Why use photodiodes ? Photodiode characteristics,and Typical applications. Also included are a complete selection guide,detailed device specifications, and package outline drawings to answer those remaining design-in questions. EG&G Vactec is a leading designer and manufacturer of dependable, cost effective opto devices and custom opto sub-assemblies. These products are used in automotive, security, scanner, lighting controls, smoe detector, X-ray detector, photographic, consumer electronics, office automation,machine controls, and medical instrumentation applications. Based in St. Louis, MO, EG&G Vactec is part of the EG&G Optoelectronicsand Components Group headquartered in Sunnyvale, CA. Parent EC&G, Inc.,Wellesley, MA, is a Fortune 200 company with annual sales of $2.7 billion.

CONTACT:
EG&G Optoelectronics, Vactec Division,
10900 Page Ave.,
St. Louis, MO 63132,
Phone: 314 423-4900, FAX: 314 423-3956.



EG&G VACTEC
PHOTODIODES

- High Performance
- Cost Effective
- High Volume
- Custom Capabilities

Choose from a wide selection of standard packages and sensitivities ■ Or, make us your design partner and let us deliver a customized solution that meets your precise needs ■ Take advantage of Vactec's years of design experience and proven high volume manufacturing capability

Applications include:

- Medical Diagnostics
- Bar Code Scanners
- Security Systems
- Cameras
- Environmental Monitoring
- Consumer Products
- Laser Detectors
- Colorimetric Analysis
- Lighting Controls
- Automotive Sensors
- Spectrophotometry
- X-Ray Detection
- Range Finders
- Encoders

Call, write or fax for the
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FAX (314) 423-3956

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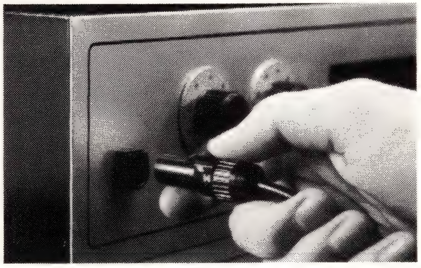
READER SERVICE 139

▼ DENSE CONNECTOR PACKS FOUR POSITIONS

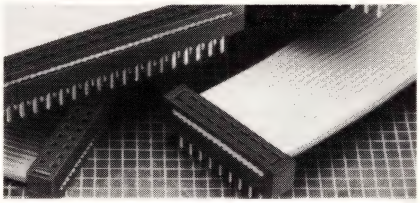
A high-density cable-to-chassis or cable-to-cable connector houses four positions for medical, process-control, and test and measurement instrumentation. The D01 Series connector features a polycarbonate housing and provides both crimp and solder-cup contacts in a compact 1.732-by-0.551-in. envelope. A push-button-style latching system eliminates field problems associated with complex and easily damaged approaches. Pricing is from $6.50 to $8 per mated pair in lots of 1000. Delivery is in from four to six weeks.



Hypertronics Corp.
16 Brent Dr.
Hudson, MA 01749
(800) 225-9228
▶ CIRCLE 638

▼ 2-MM IDC CONNECTOR OFFERS LOW PROFILE

A micro-IDC system with terminals on a 2-by-2-mm pitch is available. The double-row TCMD Series features 0.5-mm^2 phosphor-bronze pins and can be specified with two to 25 positions per row. Notch and position polarization are both available as options. The cable assembly measures just 5 mm tall when fully assembled for the lowest possible profile. The series mates with a number of the company's through-hole and SMT socket strips on 2-mm centers. Prices are as low as $0.06 per pin in lots of 1000. Delivery is typically in five working days.



Samtec Inc.
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New Albany, IN 47151-1147
(800) SAMTEC-9
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(ID) (ZI) (SM) (DP) (PG)
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San Diego, CA 92126
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RIA electronic Inc.
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Eatontown, NJ 07724
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(BB) (GP) (BM) (CN) (IN) (VR)
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(see p. 146 for key)
(continued on p. 146)

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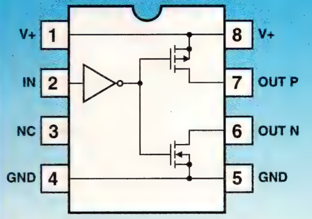
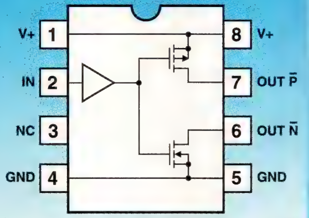


Non-Inverting
- ■ Isolated Drains
- ■ 20 ns Switching Time
- ■ $1.96 – 100's P-DIP

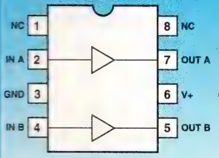
EL7114



Inverting
- ■ Isolated Drains
- ■ 20 ns Switching Time
- ■ $1.96 – 100's P-DIP

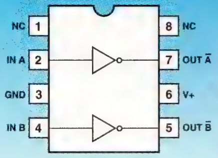
Dual Channel, 2.0 Amps Output

EL7202



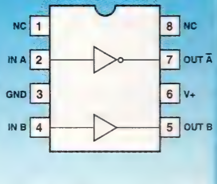
Non-Inverting
- ■ 20 ns Prop Delay
- ■ 20 ns Switch. Time
- ■ $1.55 – 100's P-DIP

EL7212



Inverting
- ■ 20 ns Prop Delay
- ■ 20 ns Switch. Time
- ■ $1.55 – 100's P-DIP

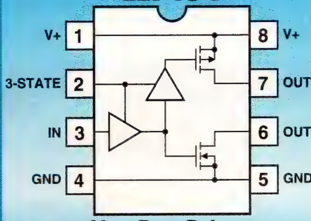
EL7222



Complementary
- ■ 20 ns Prop Delay
- ■ 20 ns Switch. Time
- ■ $1.55 – 100's P-DIP

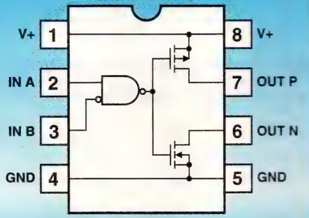
3-State Line Driver/Dual Input Line Driver, 4.0 Amps Output

EL7134



- ■ 20 ns Prop Delay
- ■ 20 ns Switching Time
- ■ $2.40 – 100's P-DIP

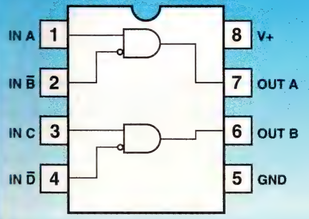
EL7144



- ■ 20 ns Prop Delay
- ■ 20 ns Switching Time
- ■ $2.40 – 100's P-DIP

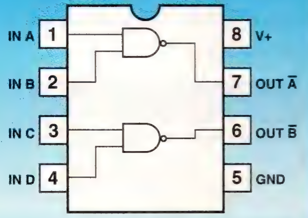
Dual Channel/Dual Input, 2.0 Amps

EL7242



- ■ 20 ns Prop Delay
- ■ 20 ns Switching Time
- ■ $2.25 – 100's P-DIP

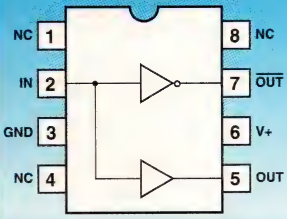
EL7252



- ■ 20 ns Prop Delay
- ■ 20 ns Switching Time
- ■ $2.25 – 100's P-DIP

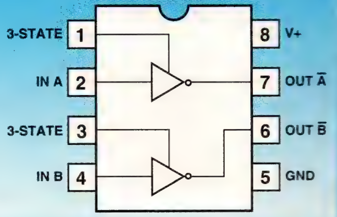
CCD Driver/Dual Channel 3-State Line Driver

EL7182



- ■ Reduced Clock Skew
- ■ 20 ns Switching Time
- ■ $2.25 – 100's P-DIP

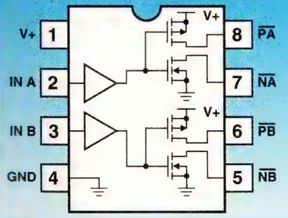
EL7232



- ■ 20 ns Prop Delay
- ■ 20 ns Switching Time
- ■ $2.25 – 100's P-DIP

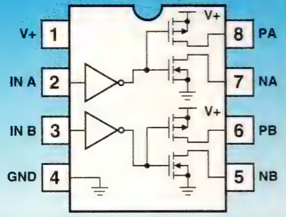
Dual Channel – Isolated Drains, 2.0 Amps

EL7262



- ■ 20 ns Prop Delay
- ■ 20 ns Switching Time
- ■ $2.25 – 100's P-DIP

EL7272



- ■ 20 ns Prop Delay
- ■ 20 ns Switching Time
- ■ $2.25 – 100's P-DIP

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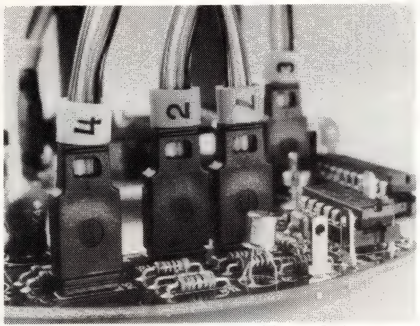
▼ 2-MM CONNECTOR BOOSTS CONTACT DENSITY



A single-row wire-to-board connector system based on the European 2-mm grid is available for high-density applications. The SP Series pc-board socket headers are offered in two through six positions and are polarized for proper mating of the male connector. A keying system prevents mismating. Male connectors have a positive lock and are supplied premolded to either jacketed cable, ribbon cable, or twisted pair in either straight or right-angle versions. An SPSG66FA six-conductor cable assembly with connector costs $3.11 in lots of 1000. Delivery is from stock to six weeks.

Richard Hirschmann of America Inc.
Industrial Row
P.O. Box 229
Riverdale, NJ 07457
(800) 225-0254, ext. 230
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▼ RAIL-MOUNTED HEADER SAVES SPACE

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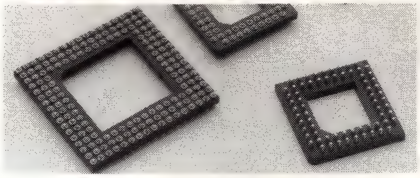
▶ **CIRCLE 641**

▼ PGA SOCKETS FEATURE FLOATING PINS



A series of pin-grid-array sockets for surface mounting feature pins with 0.005 to 0.009 in. of float, which allows for board warpage during soldering without disturbing solder-joint integrity. The SM sockets is made with FR-4 or 0.110-in.-thick high-temperature plastic. The sockets' precision screw-machine contacts offer tapered entry for easy device insertion. Contact resistance is 10 mΩ maximum with insulation resistance of 5000 MΩ at 500 V dc. Prices range from $0.030 per pin in lots of 1000. Delivery is in four to six weeks.

Garry Electronics
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23 Front St.
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Tricon Industries Inc.
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Lisle, IL 60532-2167
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Westlake Village, CA 91362
(818) 707-2020
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(508) 532-0775

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(FO)
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Liverpool, NY 13088
(315) 451-7807
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Yamaichi Electronics Inc.
1420 Koll Circle, Suite B
San Jose, CA 95112
(408) 452-0797
CIRCLE 921

Zierick Manufacturing
Research & Development
Radio Circle
Mt. Kisco, NY 10549
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(AU) (RF) (CX) (ID)
(ZI) (SM) (CD) (RP)
CIRCLE 922

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Van Nuys, CA 91406
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(EM) (CM)
CIRCLE 923

KEY

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(AU)	Audio
(RF)	Radio-frequency
(CX)	Coaxial
(DS)	D-subminiature
(DI)	DIN design
(EL)	Elastomeric
(FC)	Flat cable
(CE)	Card edge
(ID)	Insulation displacement
(ZI)	Zero/low insertion force
(SM)	Surface mountable
(CC)	Chip carriers
(DP)	DIP/SIP
(PG)	Pin-grid array
(CD)	Custom design
(MD)	Military design
(BI)	Test and burn-in
(HV)	High-voltage
(HC)	High-current
(RP)	Rack-and-panel
(FO)	Fiber optic
(TE)	Terminal blocks

Boards and Panels

(SS)	One-sided
(DD)	Double-sided
(ML)	Multilayer
(WR)	Wire-wrap
(FX)	Flexible
(BP)	Backplane
(PC)	Printed circuit
(VB)	VME bus
(SB)	Standard bus
(MB)	Multibus
(IB)	IBM PC bus
(BU)	Futurebus
(GB)	Other bus

Wire and Cable

(CO)	Coaxial
(FL)	Flat
(TW)	Twisted-pair
(SH)	Shielded
(WV)	Woven
(PW)	Power cords/cables
(MN)	Magnet wire
(HK)	Hookup wire
(HN)	Harnesses
(CA)	Cabling materials
(BB)	Bus bars

Enclosures

(GP)	General purpose
(BM)	Bench-mounted
(CN)	Consoles
(IN)	Instrument cases
(VR)	Vertical racks
(WT)	Water-tight
(PT)	Portable
(EM)	EMI/RFI design
(MI)	Military design
(CM)	Custom design

Shielding

(ES)	Electrostatic
(MG)	Magnetic
(ER)	EMI/RFI
(GK)	Gasket
(FR)	Ferrites
(SE)	Sheets/strips
(TB)	Tubing
(RC)	Rooms and chambers
(VE)	Vents
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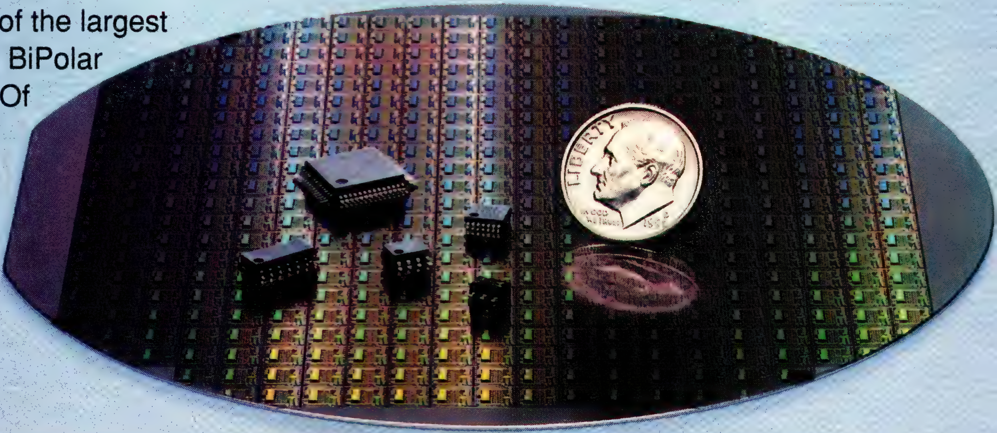

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NJU3714	12-bit Serial In Parallel Out with Cascade Function	D, G20
NJU3715	16-bit Serial In Parallel Out	L, G22
NJU3716	16-bit Serial In Parallel Out with Cascade Function	L, DMP24
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NJU3719	24-bit Serial In Parallel Out	L15

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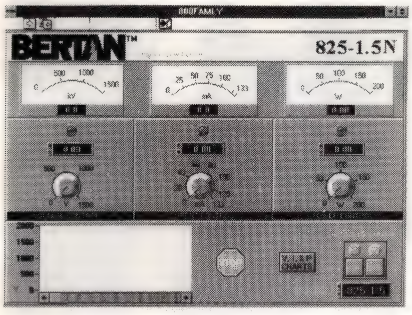
READER SERVICE 16

▼ HIGH-VOLTAGE SUPPLIES ARE CONTROLLED BY PC

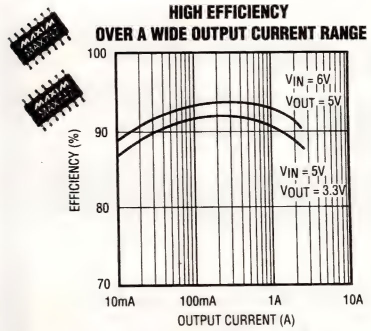
Outputs of 100, 200, or 300 W are available in a line of computer-controlled, high-voltage switching power supplies. The Series 800 supplies offer voltage outputs ranging from zero to 500 V to zero to 60 kV. A complete system includes a supply, a data-acquisition card, LabVIEW for Windows software, and the appropriate software drivers. With this system and an IBM-compatible PC, complete, user-friendly control and monitoring is possible for all power-supply parameters. The virtual-instrument front panel allows users to access features interactively. Call for pricing and delivery.



Bertan High Voltage
121 New South Rd.
Hicksville, NY 11801
(800) 966-2776
▶CIRCLE 643

▼ 5-TO-3.3-V CONVERTER KEEPS PCs GREEN

Two low-cost ICs provide highly efficient, high-current step-down regulation at low input and output voltages. The MAX746 and MAX747 converters are well suited for 5-V-input/3.3-V-output "green-PC" and other step-down applications. Typical efficiency for such uses is 88% to 92% for loads of 10 mA to 2.5 A. The output also can be adjusted from 2 V to 14.5 V. The MAX746 drives an external n-channel MOSFET on the high side and comes in 16-pin narrow SOICs and DIPs. The MAX747 drives an external p-channel MOSFET and comes in 14-pin narrow SOICs and DIPs. Prices for both start at $2.25 in lots of 1000.



Maxim Integrated Products
120 San Gabriel Dr.
Sunnyvale, CA 94086
(408) 737-7600
▶CIRCLE 644

▼ WIDE-RANGE CONVERTER DELIVERS FULL 5 W

Input voltages of 18 to 36 V dc or 36 to 72 V dc are offered in the WP05R Series of wide-range dc-dc converters. Available standard outputs include 5, 12, 15, ±5, ±12, and ±15 V dc. All models supply a full 5 W and come in a small 1-by-2-in. package. Units operate at full power up to +70°C without a heat sink. With minimal airflow, operation is to +85°C at full load. All incorporate a 500-V dc isolation barrier and have internal continous short-circuit protection. Call for pricing and delivery.

Powr Convertibles Corp.
Burr-Brown
3450 S. Broadmont Dr.,
Suite 128
Tucson, AZ 85713
(602) 628-8292
▶CIRCLE 645

▼ NiMH-BATTERY LINE INCLUDES PRISMATICS

A rectangular (prismatic) nickel metal hydride battery is available with a nominal voltage of 1.2 V. The HHF80T cell measures 17 mm long, 6.1 mm wide, and 67 mm tall. It weighs about 25 grams and features a nominal capacity of 760 mAh. The batteries' one-hour recharge capability, stable discharge characteristics, and reliability make them suitable for personal digital assistants, some cellular mobile telecom applications, and other uses in which high energy density and small size are critical. Call for complete pricing and delivery information.

Panasonic Industrial Co.
Two Panasonic Way
Secaucus, NJ 07094
(800) 848-3979
▶CIRCLE 646

▼ TRIPLE-OUTPUT SUPPLY AIDS IN DESIGN, TEST

High performance and reliability for designing, testing, and repairing precision digital and analog circuits is provided by the HP 3630A triple-output dc power supply. The 35-W unit's outputs are zero to 6 V with a maximum current of 1 to 2.5 A and zero to –20 V and zero to –20 V with a maximum current of 0.5 A. Normal-mode noise is specified at less than 0.35 mV and common-mode current is specified at less than 1 μA. Line and load regulation of 0.01% keeps outputs steady with changes of the power line and load. Pricing is $500 each with delivery from stock.

Hewlett-Packard Co.
Direct Marketing
P.O. Box 58059, MS51 L-SJ
Santa Clara, CA 95051-8059
(800) 452-4844, ext. 7941
▶CIRCLE 647

▼ UNIVERSAL FRONT END POWERS SUPPLIES OFF-LINE

A universal ac front end is claimed as the only modular auto-ranging front end available, allowing designers to operate dc-dc converters off-line on either a 115- or 230-V ac input. The UNV300 front end can be used with any dc-dc converter that accepts a nominal 300 V dc (200 to 400 V dc) input. No manual strapping is required. The front end senses the input voltage and automatically configures itself for an 85-to-135-V ac input (voltage-doubler mode) or a 180-to-265-V ac input (bridge-rectifier mode). Pricing is $130 each in OEM quantities.

Powercube Corp.
Eight Suburban Park Dr.
Billerica, MA 01821
(508) 667-9500
▶CIRCLE 648

IT'S P-P-PERFECT.
IT'S DREADFUL!

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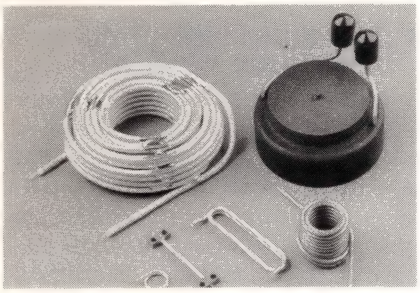
A public service of this magazine

▼ CUSTOM DELAY LINES SERVE WIRELESS NEEDS

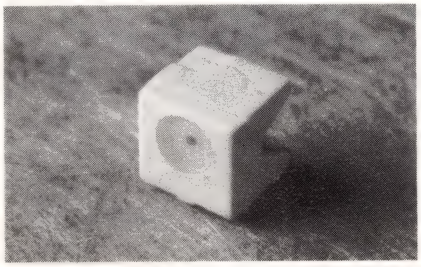
A complete line of compact custom delay lines is designed to meet the requirements of cellular, paging, land mobile, and other wireless applications. A wide variety of delay times is offered with superior insertion-loss characteristics. Standard delay times range from 1 to 200 ns with insertion loss ranging from 1.2 to 5.9 dB at 900 MHz. Dimensions range fromm 0.75 in. high by 1 in. diameter to 2.25 in. high by 2.75 in. diameter. Call for pricing and delivery.



Micro-Coax
Box 993, 245 W. 5th Ave.
Collegeville, PA 19426-0993
(215) 489-3700
▶ CIRCLE 649

▼ RIGHT-ANGLE SMT LED CUTS DESIGN TIME

Ten versions of the SIDELED, a true right-angle, surface-mounted LED, mount so that the light emission is parallel to the pc board. The devices, which are additions to the SMT-TOP-LED family, include two emitters and one phototransistor (detector) for infrared applications. Seven colors are offered for visible-light uses. The LEDs ease the design process by giving designers more flexibility in that designs may be completed before the need for a right-angle LED lamp has been determined. The 4-mm-tall LEDs are the same height as standard ICs. As an example, pricing for the yellow, orange, super-red, and green visible-light versions is $0.24 in lots of 10,000. Samples are available now.



Siemens Optoelectronics Div.
2191 Laurelwood Rd.
Santa Clara, CA 95054
(800) 777-4363
▶ CIRCLE 650

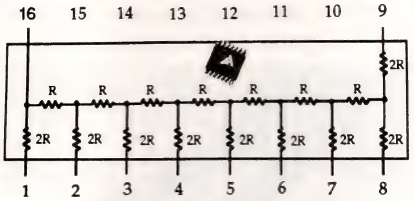
▼ MICA CAPACITORS HANDLE HIGH dV/dTs

The Snubber Mike silvered-mica capacitors now offer dV/dT ratings of more than 100,000 V/µs. With five times the peak current capability of earlier versions, the Snubber Mikes are a reliable choice for high dV/dT snubber circuits and resonant power supplies. The devices handle up to 3700 A of peak current and 8.7 A of continuous current. With their ultra-stable mica dielectric, changes in capacitance with voltage, temperature, or frequency are unmeasurable. Values range from 100 pF to 0.01 µF and voltages from 500 to 1500 V dc. Pricing is from $0.15 in lots of 1000. Delivery is from stock to 12 weeks.

Cornell Dubilier
1605 Rodney French Blvd.
New Bedford, MA 02744
(508) 996-8564
▶ CIRCLE 651

▼ R-2R LADDER NETWORK IS FULLY INTEGRATED

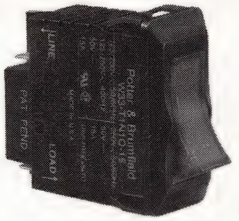
An integrated R-2R precision ladder-network product line has joined the Integrated Passive Electronic Components (IPEC) family of devices. The network combines 16 resistors in a standard ladder configuration in space-saving 25- or 50-mil SMT packages. This format gives designers board-space reductions of over 50% compared with conventional discrete, thick-film R-2R ladder implementations. Standard values are 10 kΩ, 25 kΩ, and 50 kΩ in each package format. Pricing, in lots of 10,000, ranges from $1.35 to $2 depending on package. Delivery is in six weeks.



California Micro Devices Corp.
215 Topaz St.
Milpitas, CA 95035-5430
(408) 263-3214
▶ CIRCLE 652

More quality switching components from P&B

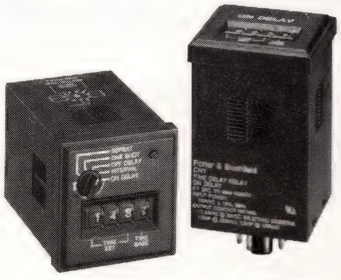
W33 Thermal Circuit Breaker



One- or two-pole sensing, two-pole breaking model offers current ratings from 5 through 20A. W33 provides circuit protection, on/off switching and an optional indicator lamp in a single, compact package. Snaps into panel cutout without tools. Designed to meet international standards.

READER SERVICE 120

CN1/CNM5 Time Delay Relays



Low-cost units time from 0.1 sec. to 9,990 hrs. with digital accuracy. CN1 is an on-delay timer. CNM5 provides five different timing functions. Each model is housed in a 1/16 DIN enclosures and has a DPDT output relay rated 10A @ 240VAC. 8-pin (CN1) or 11-pin (CNM5) plug-in base.

READER SERVICE 182

W6 Magnetic Circuit Breaker

VDE APPROVED MODELS NOW AVAILABLE

Breaker is offered in one- through four-pole models for current ratings from 200mA through 50A. Recent line extensions include snap-mount models and types with single actuators for multiple poles. Series offers various trip-time delays, circuit functions, mountings and actuator options.

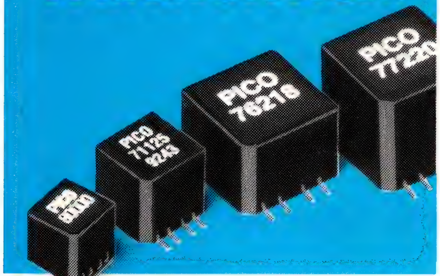
Potter & Brumfield
A Siemens Company

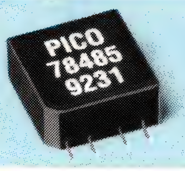
READER SERVICE 183

9401

PICO

U L T R A - M I N I A T U R E
Surface Mount
Audio
Transformers





Low Profile
.2" Ht.

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- Operating temperature –55°C to +130°C
- Low profile .2" ht.

PICO surface mount units utilize materials and methods to withstand extreme temperature (220°C) of vapor phase, I.R., and other reflow procedures without degradation of electrical or mechanical characteristics.

Delivery—stock to one week

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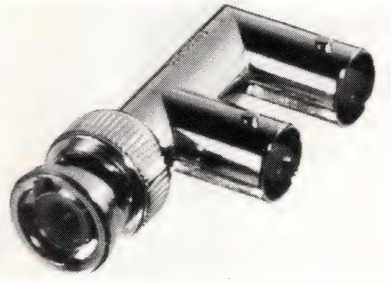
in NY call **914-699-5514**
FAX **914-699-5565**

PICO Electronics, Inc.
453 N. MacQuesten Pkwy., Mt. Vernon, N.Y. 10552

READER SERVICE 188

▼ THREE-PORT ADAPTER NEATENS NET CABLING

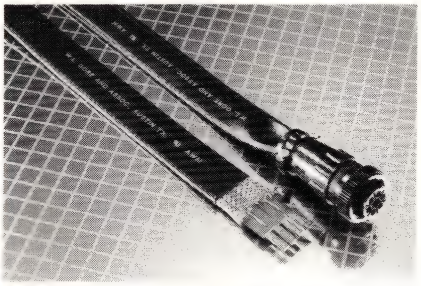
Two BNC three-port adapters made in the shape of the letter F take the place of a standard BNC T connector. The two-female and one-male adapters allow connection directly to an Ethernet LAN card and to two network coaxial cables, which can be neatly strapped together and run to a wallplate. With a T adapter, the cables diverge in opposite directions and it's harder to keep them neat. The RFB-1130-3 adapter is a 50-Ω version for LAN and RF applications, while the RFB-1730-3 is a 75-Ω part for CATV and video cables. Both are delivered from distributor stock. Call for pricing.



RF Industries Ltd.
7620 Miramar Rd.
San Diego, CA 92126
(800) 233-1728
▶ CIRCLE 653

▼ FLEXIBLE CABLE CARRIES HIGH POWER

A family of shielded power cables is designed to reduced non-scheduled maintenance of industrial power supplies. The cable packages groups of three or four conductors laid in parallel to form a low-profile, more flexible cable pod. The cables are rated at 600 V at 60°C and are equivalent to bulkier, single-conductor, large-gauge designs. PTFE insulation is used for a low coefficient of friction, which in turn provides a long flex life. Braided copper shielding gives high electrical isolation. Call for pricing and delivery.



W.L. Gore & Associates Inc.
7811 Burleson-Manor Rd.
Manor, TX 78653
(800) 531-6064
▶ CIRCLE 654

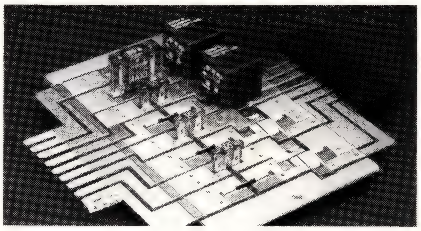
▼ STACKING CONNECTORS BOAST LOW PROFILE

A range of low-profile, surface-mounted connectors is available to assist in downsizing computer and telecommunication products. The Conan microminiature connector system starts with an ultra-low profile of 4.15 mm and also offers mating heights of 4.5, 5, 6, and 7 mm. This flexibility permits increasing clearances between parallel boards to accommodate larger components. The connectors may also be used on flexible circuits. A 1-mm contact pitch provides a contact density of 50/linear inch. Call for pricing and delivery.

Berg Electronics Inc.
825 Old Trail Rd.
Etters, PA 17319
(800) 237-BERG
▶ CIRCLE 655

▼ FUSE-PLANE SYSTEM DISTRIBUTES POWER

A power-distribution system allows the integration of blade-type fuses and other components. The Excor fuse-plane system enables fuse systems, relays, breakers, and connectors to be mounted and interconnected directly to the planar component for a simpler, more reliable power-distribution package. The system adds the blade-type component mounting and interconnecting capability to the existing Excor line, which combines consistent electrical performance and design flexibility in a space-saving assembly. Call for pricing and delivery.



Rogers Corp.
Power Distribution Div.
5750 E. McKellips Rd.
Mesa, AZ 85205
(602) 641-6660
▶ CIRCLE 656

▼ IC SOCKETS STAR IN BROAD CATALOG

Numerous types of IC sockets, pc-board connectors, jumpers, and headers are described in detail in Catalog 10P. The 72-page catalog kicks off with a quick-selector chart that lets engineers settle on an insulator and pin style and then points them to a specific section within the catalog for more information. Complete dimensional diagrams are supplemented with mechanical, electrical, and environmental data for all products. Also included is a wide array of pin-grid sockets.

Mill-Max Mfg. Corp.
190 Pine Hollow Rd.
P.O. Box 300
Oyster Bay, NY 11771-9918
(516) 922-6000
▶CIRCLE 657

▼ TEST/BURN-IN SOCKETS HANDLE FINE PITCHES

An extensive range of sockets for test and burn-in of surface-mounted devices, fine-pitch products, and molded carrier rings are detailed in a 40-page catalog. Included are the company's 7000 Series TQFP sockets, which are compatible with multiple device thicknesses of 1 and 1.4 mm. Also covered are a full line of 0.5- and 0.65-mm-pitch molded-carrier-ring sockets. The 550/560 Series sockets meet Jedec specifications and feature standard footprints. Profusely illustrated, the catalog contains complete technical data and dimensional drawings for all products.

CTi Technologies Inc.
7855 E. Evans Rd., Suite A
Scottsdale, AZ 85260
(602) 998-1484
▶CIRCLE 658

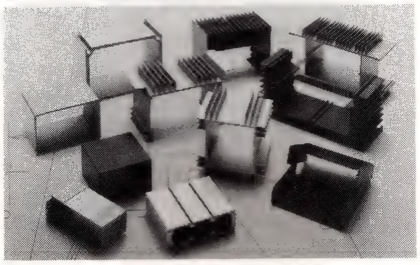
▼ ENGINEERING CATALOG SHOWS MANY CONNECTORS

A large, full-line catalog contains complete engineering information on a broad assortment of interconnections including 2-mm dual row connectors and headers, wire-to-board and board-to-board connectors, card-edge types, SIMM sockets, IDCs, SMT types, and many more. This engineer's resource details hundreds of interconnections for virtually any application. Descriptions of the products' features are supplemented by full performance specifications and dimensional drawings.

Methode Electronics Inc.
7444 W. Wilson Ave.
Chicago, IL 60656
(708) 867-9600
▶CIRCLE 659

▼ TECHNICAL GUIDE HELPS ENCLOSURE USERS

A brochure offering technical assistance in designing aluminum electronic enclosures is available. A wide variety of design suggestions as well as specific details for drawing layouts are included. The brochure points out ways to reduce costs, improve the enclosure's appearance, and extend the system's life. Also offered are multi-functional solutions that allow designers to perform enclosure layouts with an emphasis on mechanical as well as thermal characteristics.



Aavid Engineering Inc.
One Kool Path, P.O. Box 400
Laconia, NH 03247-0400
(603) 528-3400
▶CIRCLE 660

▼ CONNECTOR SOURCEBOOK COMES IN TWO VERSIONS

For the first time, two separate versions are available of the 1993/1994 Connector Sourcebook catalog from ITT Cannon. One version covers commercial and industrial products, while the other spans military and aerospace products. This format change streamlines users' search for the most appropriate connector solution for their applications. The catalogs' index is cross-referenced by part numbers and product descriptions. Both are profusely illustrated with technical drawings, dimensional diagrams, and photographs.

ITT Cannon
1851 E. Deere Ave.
Santa Ana, CA 92705
(714) 757-8415
▶CIRCLE 661

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ENGINEERING, INC.
1636 Hyde Park Ave.
Hyde Park, MA 02136

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READER SERVICE 85

Because you're thinking fast...

First we cut noise, distortion, settling time and power. Now...

Now we've made big cuts in prices too. Recent reductions in our op amp family averaged 25%, which means you get exceptional performance for your money. That applies to the newest additions to our low-noise, voltage-feedback op amp family too. For example:

200MHz GBW, 1.6nV/√Hz voltage noise, $4.75*.

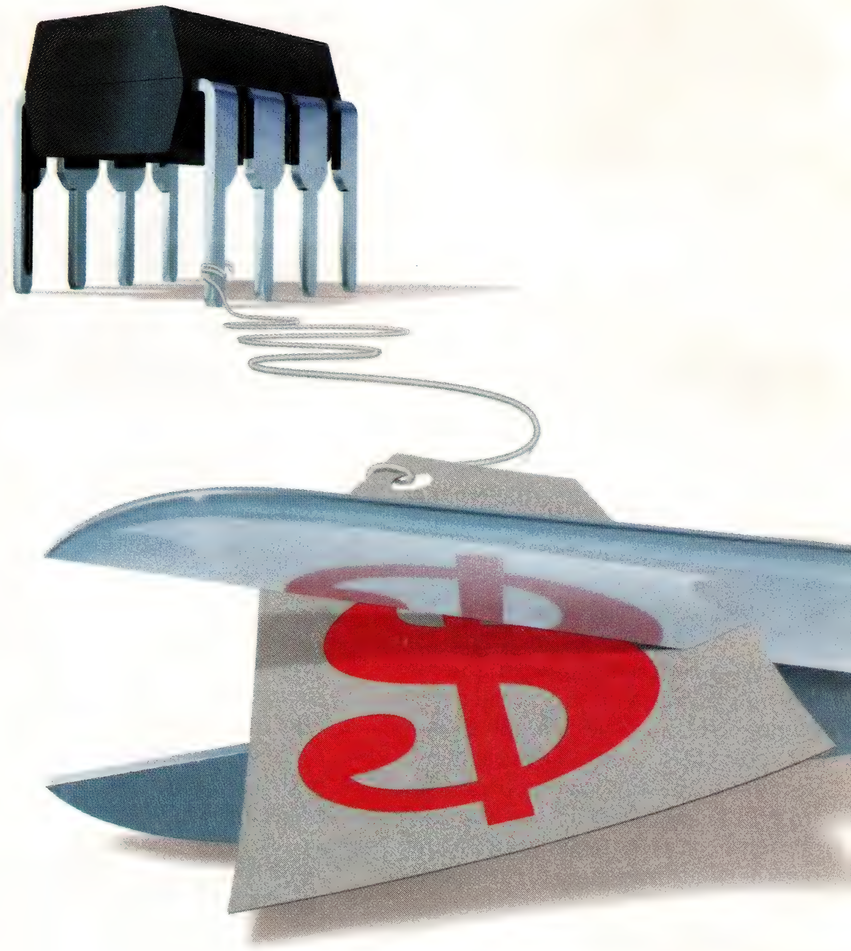
Our new CLC426 couples high gain-bandwidth and low noise with a fast 700V/µs slew rate and 30ns settling time (0.01%). You get low distortion and adjustable supply current too. It's priced right for applications like wideband low-noise integrators, input buffers for hi-resolution A/Ds and other signal-conditioning applications requiring the combination of speed, low noise, low distortion and low dc errors.

Dual high-BW, low-noise op amp for $7.12*.

In a class by itself, the new CLC428 packs two unity gain stable, 140MHz GBW op amps with 2.0nV/√Hz voltage noise in the same package. This leading-edge device also features a fast 400V/µs slew rate and 30ns settling time to 0.01%. This dual op amp offers great performance for the price and is ideal for multichannel integrator applications such as state-variable filters.

Don't cut yourself out of the best deals in op amps. Call today and find out just how much performance you can get for the money.

READER SERVICE 145



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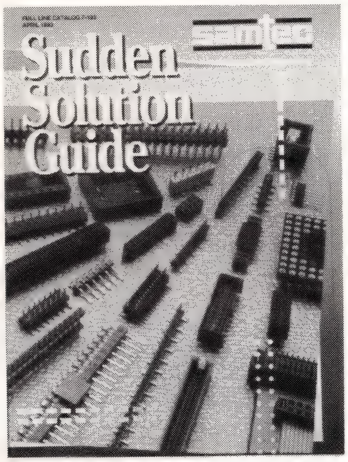
▼ FULL CONNECTOR LINE DETAILED IN CATALOG

Complete ordering information and specifications on many new interconnects are contained within the full-line catalog F-193. Micro connectors, SMT products, board-to-board interconnects, sockets and adaptors, IDC cable assemblies, elastomeric connectors, and custom design capabilities are described. A 16-page applications section provides details on SMT systems, specific application examples for standard and custom interconnects, design for manufacturability, and quality programs.



Samtec Inc.
P.O. Box 1147
New Albany, IN 47151-1147
(800) SAMTEC-9
▶ CIRCLE 662

▼ CAPACITOR CATALOG BOASTS BROAD RANGE

A wide selection of capacitors from aluminum electrolytics, solid tantalums, and ceramic-disc types to mylar/polyester film and motor-run and motor-start types is offered in a catalog from NTE Electronics. Detailed specifications and case sizes and dimensions are clearly spelled out. A particularly useful feature is a section on recommended cleaning solvents for each type.

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(800) 631-1250
▶ CIRCLE 663

▼ DIN 41612 GUIDE COVERS CONNECTORS

A 52-page, four-color catalog covers ERNI's full line of DIN connectors incorporating the internationally accepted design advantages of DIN 41612/IEC 603-2. The line is organized into six categories: standard DIN, inverse DIN, low-profile power types, heavy-duty power types, high current, and hybrid types for power and signal. Full product data is supplemented by clear, easy-to-read diagrams, application information, and design considerations.

ERNI Components Inc.
520 Southlake Blvd.
Richmond, VA 23236
(8004) 794-6367
▶ CIRCLE 664

▼ GUIDE SUPPORTS OSCILLATOR USERS

An expanded user's guide to quartz crystals and oscillators offers complete information on a large range of timing devices. Included are full technical descriptions on products such as low-frequency crystals, microprocessor types, MIL-spec crystals, crystal clock oscillators for TTL, ECL, and CMOS logic, high-temperature oscillators, and many more. The catalog is brimming with drawings, specifications, and application information. A helpful guide to terms and definitions is also offered.

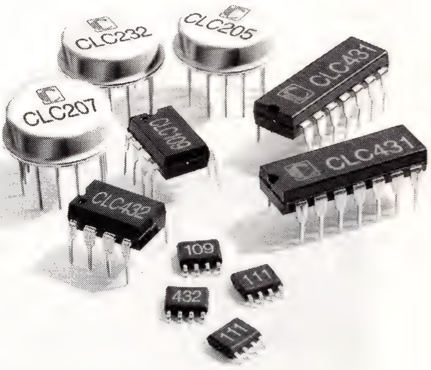
Valpey-Fisher Corp.
75 South St.
Hopkinton, MA 01748
(508) 435-6831
▶ CIRCLE 665

▼ SMD FERRITES IN EXPANDED RANGE

Surface-mounted ferrites are the subject of a catalog from Siemens Components. An up-to-date survey of the company's offerings includes ready-wound SMD transformers plus ferrites and accessories as components for SMD inductors. The range of transformers has been expanded and covers the entire selection of preferred products including designs P 4.5, E 6.3, ER 11, RM 4LP, and RM 5. Transformers can also be custom wound to meet the specifications of any application.

Siemens Components
Ferrite Product Mktg.
Special Products Div.
186 Wood Ave. South
Iselin, NJ 08830
(800) 888-7728
▶ CIRCLE 666

Bargain buffers and wideband op amps.



Fast buffers use little power. Pick from two new closed-loop, unity-gain buffers for video switch buffers, testpoint drivers and very high-speed active filters. The 270MHz CLC109 delivers a 350V/µs slew rate at just 3.5mA (± 5V). And just for $1.49*. The 800MHz CLC111 slews at a blazing 3500V/µs at 10.5mA. And it's only $2.75*.

READER SERVICE 146

Dual op amps also combine speed, low power. For dual selectable-gain amplifiers, video signal multiplexing and a host of amplifier and driver applications, pick the 62MHz CLC431(with disable input) or the CLC432. They take 7mA/Amp, slew at 2000V/µs, support video specs and operate on ±5 to ±15V supplies. Priced at just $2.99* and $2.49* respectively.

READER SERVICE 184

Prices cut on ultra-high-performance hybrids. Need great distortion specs for fast, precision ADs and receiver IF stages? How about high output swing? Check the prices on our 170 MHz, high-gain CLC205 and CLC207. And the low gain, 270MHz CLC232. All three combine high speed with ultra low distortion. And prices start at just $24.50*.

*U.S. list price in 1,000s.

READER SERVICE 185

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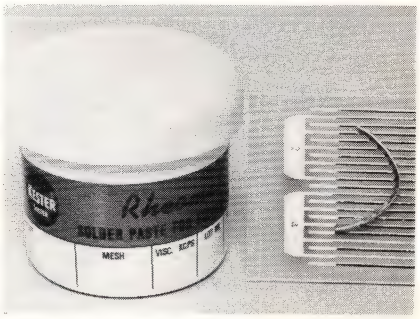
▼ GREEN-TAPE SYSTEM LOWERS MCM COSTS

Multichip-module manufacturers can make low-cost, high-conductivity circuits with bare silicon ICs using a low-temperature cofired ceramic system from DuPont. The 901 Green Tape system is a cordierite, crystallizable, glass-filled tape dielectic material that's compatible with copper or gold conductors and processed in simple, single-atmosphere firing profiles. The material's low dielectric constant (5.2) and TCE matched to silicon (3.2) makes it well suited for bare ICs in multichip formats. Call for pricing and delivery.

DuPont Electronic Materials
Barley Mill Plaza, Room G-52198
Wilmington, DE 19880-0010
(800) 237-4357
▶CIRCLE 667

▼ NO-CLEAN SOLDER IMPROVES TESTABILITY

A no-clean solder paste for nitrogen-atmosphere reflow applications significantly improves electrical testing of boards, which is sometimes hampered by the presence of solder residue. The R-215 low-residue solder paste leaves boards with a shiny, clean appearance. The material's excellent slump-resistant characteristics permits it to flow in a stable, solid form and keep its shape on the board, permitting greater component density. It can be printed down to a 20-mil pitch or lower with ultrafine powders. Call for pricing.

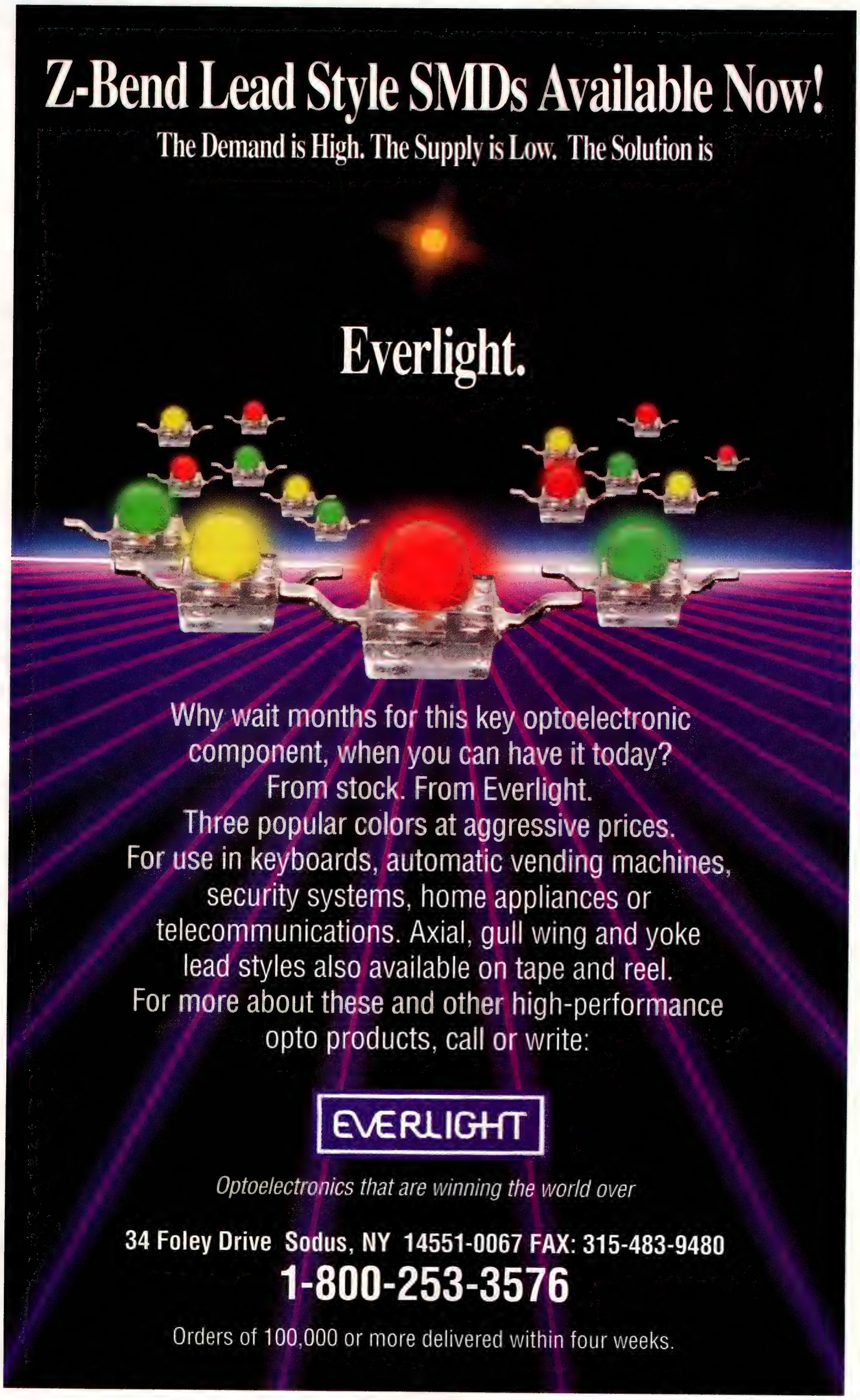


Litton Industries Inc.
360 N. Crescent Dr.
Beverly Hills, CA 90210-4867
(310) 859-5162
▶CIRCLE 668

▼ RARE-EARTH MAGNETS HAVE HIGH REMANENCE

Two powerful permanent-magnet grades have been developed on a neodymium-iron-boron base. The Vacodym 344 grade achieves a typical remanence (B_r) of 13.6 kG and offers a improved value of coercivity. With an energy density of 45 MGOe and stability up to 100°C, this grade is a good choice for disk drives, speakers, and similar applications. The Vacodym 396 grade was developed specifically for applications requiring good temperature stability coupled with high remanence. Uses include motors, generators, and couplings.

Vacuumschmelze
A division of Siemens
Components Inc.
186 Wood Ave. South
Iselin, NJ 08830
(908) 494-3530
▶CIRCLE 669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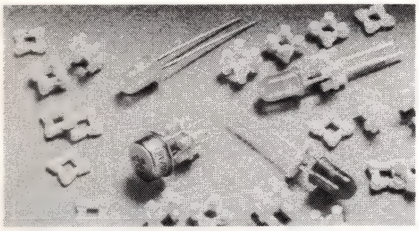
READER SERVICE 95

▼ UNIVERSAL PADS MOUNT VARIOUS LEDs

A permanent mounting pad for TO-5, TO-18, and T-1-3/4 LEDs offers simplified installation, protection during manufacturing, and reduced inventories. The 126 Series mounting pads securely mount both two- and three-lead devices, providing protection from shock, vibration, and heat.



Feet on both sides of the mounts and a totally symmetrical design makes component mounting easier without need of a specific-side or rotation orientation, allows proper board cleaning, and makes inspection faster and easier. Typical pricing is $44.50 per 1000 pieces in lots of 10,000. Delivery is from distributor stock.

Bivar Inc.
4 Thomas
Irvine, CA 92718
(714) 951-8808
▶CIRCLE 670

▼ EPOXY ADHESIVE MAKES STRONG BONDS

A two-component epoxy adhesive for structural bonding readily develops a bonding strength of more than 3000 psi at room temperature. The EP30 system has a convenient, noncritical mix ratio of 4:1 by weight or volume and is recognized for its superior resistance to thermal cycling and chemicals. Adhesion to metals, glass, ceramics, wood, vulcanized rubbers, and many plastics is excellent. Call for pricing and delivery.

Master Bond Inc.
154 Hobart St.
Hackensack, NJ 07601
(201) 343-8983
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▼ EPOXY ADHESIVE SUITS COMPONENT POTTING

An epoxy adhesive with low viscosity and black color is formulated specifically for applications such as component potting and encapsulating. Type EA9412 Black adhesive is a two-part epoxy that's pourable when mixed and is suited for injection into assembled parts. Good flexibility, high peel strength, and low-temperature properties make it practical for bonding dissimilar substrates.

Hysol Engineering Adhesives
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One Dexter Dr.
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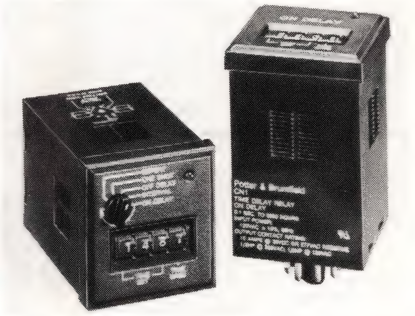
READER SERVICE 188

SWITCHES & RELAYS

▼ TIME-DELAY RELAYS BOAST HIGH ACCURACY

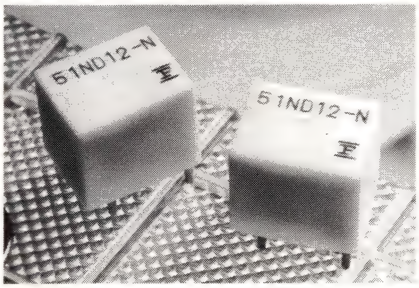
Two highly accurate, low-cost time-delay relays have been added to P&B's line. The CNM5 is a five-function programmable device, while the CN1 provides an on-delay (delay-on-operate) function. Both are housed in 1/16-DIN enclosures with round plug-in bases for socket mounting. The CNM5 has an 11-pin base while the CN1 has eight pins. Both are designed for operation on 120 V ac ±15% with a 60-Hz input. Timing is synchronized with input-voltage frequency. The products' tolerance spec of ±0.05%, ±40 ms reflects the maximum frequency variation from utility companies. The CNM5 and CN1 relays go for $52 and $42, respectively. Delivery is from stock.



Potter & Brumfield Inc.
200 S. Richland Creek Dr.
Princeton, IN 47671
(812) 386-1000
▶**CIRCLE 673**

▼ PC-BOARD RELAY HANDLES HIGH CURRENT

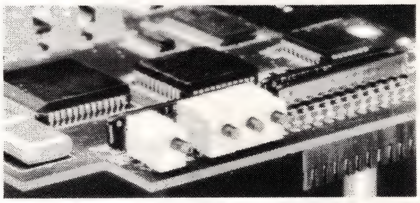
A 20-A-class automotive power relay occupies just 0.30 in.^{2} while offering a maximum carrying current of 25 A. The FBR50 Series relay has one of Fujitsu's highest contact capacities per unit volume, making it suitable not only for automotive accessories, but for any application requiring high current switching and small packaging. Features include a 1 Form C contact arrangement; 6-, 9-, or 12-V coil rating options; an operating time of 10 ms; and a 5-ms release time. Pricing for the FBR52 is $1.28 in lots of 1000.



Fujitsu Microelectronics Inc.
Electronic Components Div.
3545 N. First St.
San Jose, CA 95134
(800) 642-7616
▶**CIRCLE 674**

▼ MINI SWITCH OFFERS MANY CIRCUIT CHOICES

A small pushbutton switch provides both SPST (normally open) and SPST (normally closed) circuitry in the same package. The Series 39-714 switch also permits SPDT operation by tying terminals together. Designed to be edge-mounted on pc boards, the unit measures 0.272 in. high by 0.220 in. wide by 0.400 in. deep. An integral interlocking mechanism enables switches to be stacked side by side at the edge of a pc board. Prices are $2 in lots of 100 and $1.10 in lots of 1000. Delivery is in two weeks for prototype quantities and three to four weeks for large lots.



Grayhill Inc.
561 Hillgrove Ave.
La Grange, IL 60525
(708) 482-3132
▶**CIRCLE 675**

▼ SOLID-STATE RELAYS INCLUDE HEAT SINKS

An integral heat sink gives the PowerFin Series of SIP solid-state relays a compact, efficient package with high-power switching capability. The devices are rated at 25 A rms in forced air at an 85°C case temperature. With natural convection in free air, the relays are rated at 10 A rms at a 25°C ambient temperature. In addition, the relays offer exceptional steady state and high surge ratings thanks to the use of oversized, inverse-parallel SCR chips. Call for pricing and delivery.

Crydom Co.
6015 Obispo Ave.
Long Beach, CA 90805
(800) 8-CRYDOM
▶**CIRCLE 676**

PRODUCTS NEWSLETTER

16-Bit Stereo Chip Delivers CD Sound

Compatible with both the Microsoft Windows Sound System 2.0 standard and the Sound Blaster Pro from Creative Technologies Ltd., the ES688, a 16-bit stereo audio processor, simplifies the implementation of a generic audio subsystem. Developed by ESS Technology, Fremont, Calif., the chip includes a 16-bit stereo record and playback mode and operates at CD sample rates of up to 44.1 kHz. Also on the chip is a five-channel mixer, power-management logic, and a MIDI port. The chip can also operate from either 3.3- or 5-V supplies. Several feature settings are software selectable rather then requiring the use of wire jumpers. This makes it easier to perform board set up. Both the ADPCM and an ESS-proprietary ESPCM compression mode are supported by the chip and the circuit can directly tie into the Yamaha OPL3 sound chip to provide a full Sound Blaster Pro-compatible solution. ESS has a full demonstration library and suite of utilities to support the chip, as well as an evaluation card and sound library. In volume, the 100-lead PQFP-housed ES688 sells for less than $20 each. *DB* CIRCLE 945

Ethernet Chipset Adds To PCMCIA-Card Functions

PCMCIA cards typically make it possible for users to plug some I/O functionality, such as a fax or modem, into their portable computers. The Trio card, from Socket Communications Inc., Hayward, Calif., which fits a Type II form factor, combines an Ethernet capability with these common fax-modem functions. The ability to handle an Ethernet LAN comes from the AT&T Microelectronics Outrigger T7232 chip set. In addition to the Ethernet controller, the T7232 contains an access-unit interface (AUI), a twisted-pair transceiver, a Manchester encoder-decoder, and a PCMCIA bus interface. The Trio's modem runs at 14.4 kbits/s. The multifunction PCMCIA card is priced at $695. For information on the card, contact Socket Communications at (800) 552-3300. Chip set information is available directly from AT&T Microelectronics, Allentown, Pa. It sells for under $20 each, in lots of 50,000. The company can be reached at (800) 372-2447, Dept. P02, or (800) 553-2448 in Canada. *RN* CIRCLE 946

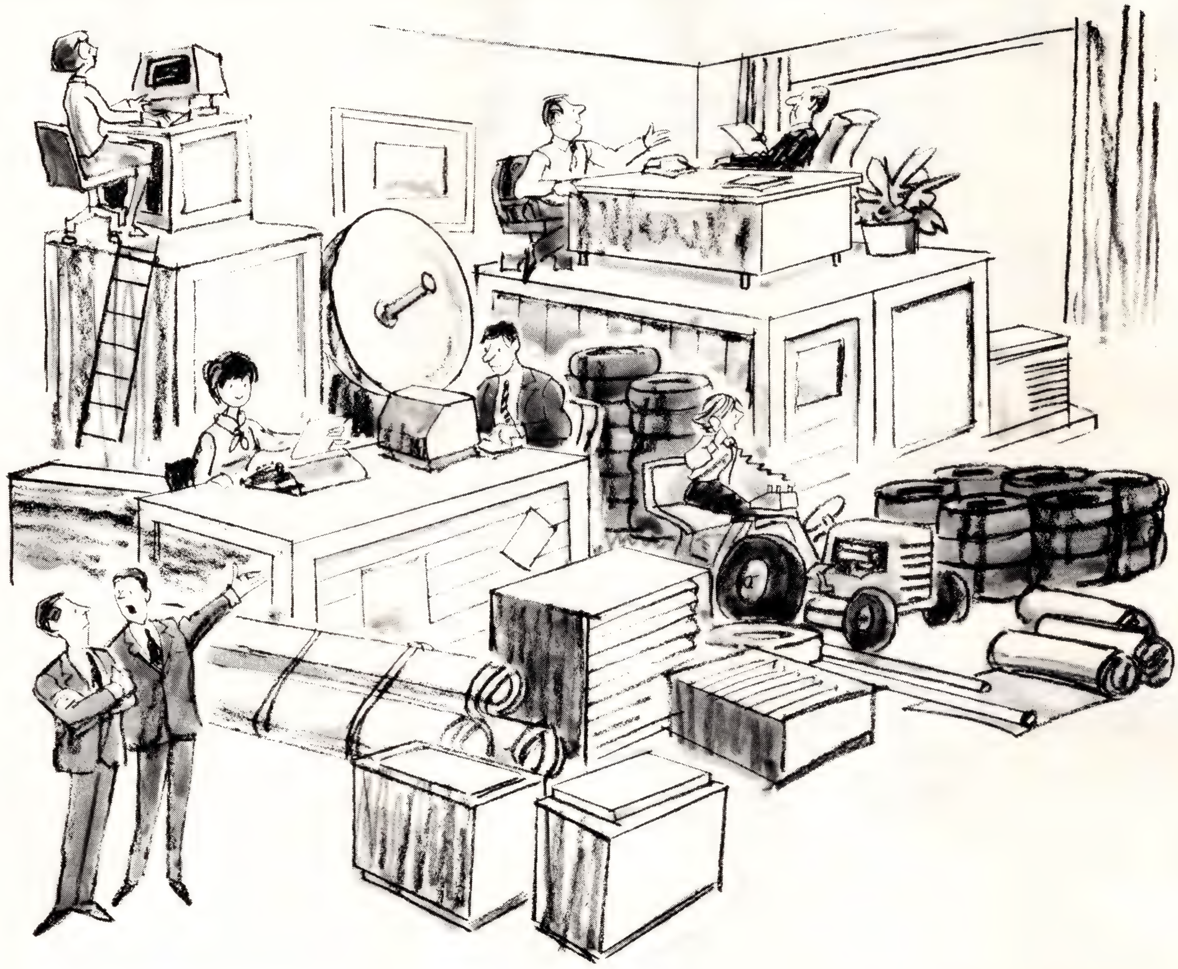
Let Host Handle Print Computations

Using the WinStyler hardware-software combination, designers can envision 600-dot/in. laser printers, capable of running in a Windows or Macintosh environment, with street prices under $700. Moreover, the WinStyler, developed by Destiny Technology Corp., Santa Clara, Calif., can drastically improve the printer performance by shifting the computational burden. Because today's PCs are typically built with 33- or 66-MHz 486 microprocessors, the PC may be better suited than the printer itself to handle the printer's computations, such as imaging and rasterizing operations. Because the imaging is handled by the host, the problems associated with the various printer languages are reduced. In addition, high-speed print jobs in both the Windows and Macintosh environments can be processed simultaneously by the WinStyler ASIC (called the QuickASIC). The graphical-device interface (GDI) software can rasterize and send 600-dot/in. images to the printer at speeds commonly associated with 300-dot/in. data, which is less complex. Because the bulk of processing is done on the host PC, the platform can perform previously unavailable functions. This is where the software comes in: Rather than have users rely on the simple interface offered by the printer, all communications between the user and printer can be handled through the PC, producing the GDI. Standalone printers based on the WinStyler technology should be available in the second or third quarter, followed by networked units later in the year. Call Destiny at (408) 562-1000. *RN* CIRCLE 947

Transceiver Supports PC And Macintosh Interfaces

A new programmable serial transceiver is one of the first that can be configured to work with either PCs or Macintosh equipment. The single-chip SP303 from Sipex Corp., Billerica, Calif., can be programmed to handle either RS-232 or AppleTalk serial interfaces, and it provides four RS-232 driver/receiver pairs in the RS-232 mode. Both a single-ended driver and receiver, as well as a differential driver and receiver, are provided in the Macintosh mode. To tie into an AppleTalk network, a driver pin on the chip can be enabled to provide for networking capabilities. The SP303 comes in a 28-lead SOIC package and is available from stock. Call the company at (508) 667-8700. *CA* CIRCLE 948

Edited by Clifford Meth



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HALF-MICRON CMOS ASICS CONTAIN UP TO 1.5 MGATES AND RUN AT 3 V

An enhanced 0.5-µm CMOS process with effective gate lengths of just 0.35 µm has been optimized by LSI Logic for 3-V operation and high density. With that process, the company has created the 500K portfolio of ASIC choices that give system designers integration levels of up to 1.5 million usable gates per chip (about 9 million transistors). The ASIC library and support tools allow designers to create chips that can operate at system speeds of up to 200 MHz (internal toggle rates of up to 400 MHz). Consequently, the 500K family delivers about a 15% to 20% performance improvement over previous 5-V offerings, in addition to the lower per-gate operating power levels.

To operate at such high speeds, the ASICs can interface with a variety of high-speed logic families: positive-referenced ECL or CML, NTL for point-to-point interconnections as fast as 622 Mbits/s, and bus interfaces in excess of 200 MHz. The I/O buffers can also provide popular CMOS and TTL interface options. With the high densities, the 500K family can deliver system-on-a-chip solutions in applications such as single-chip network routers, personal digital assistants, and graphics I/O controllers.

The high densities per chip are achieved through a combination of the optimized process and cell libraries, and up to four levels of metal interconnections, which permits high routing efficiency and high gate utilization. Furthermore, as part of the ASIC library, LSI has created even lower-voltage (2.4 V) cells, which can be mixed on the same chip with 3.3-V logic, thanks to the company's hierarchical design tool methodology.

Included in the 500K portfolio are the LCA500K family of masterslice gate arrays, the LEA500K embedded arrays, and the LCB standard-cell family. The LCA500K arrays host up to 1 million usable gates, up to 160 kbits of RAM, or 1.2 Mbits of ROM and some logic; the LCB option allows up to 1.5 million gates per chip, up to 2 Mbits of SRAM, or 6 Mbits of ROM and some logic. The LEA series has the same density capabilities as the LCB option. Packaging options include various fine-lead-pitch packages, such as ball-grid array with over 700 contacts, as well as chip-on-tape and QFPs. For test purposes, the 500K portfolio includes automatic scan and JTAG insertion and automatic boundary-scan description-language generation. Large SRAM embedded blocks include built-in self-test logic.

Non-recurring engineering charges start at $30,000. Upgrades to the company's simulation and verification tools now let the tools handle the higher complexities of the 500K family. The design library and samples are now available, with production silicon available in the third quarter of 1994.

LSI Logic Corp., 1551 McCarthy Blvd., Milpitas, CA 95035; (408) 433-8000. **CIRCLE 680**

■ *DAVE BURSKY*

EIGHT-CHANNEL UART HITS 33-MHZ BUS RATES

An eight-channel CMOS universal asynchronous receiver-transmitter (UART), the SC68C198/26C198, has been specifically optimized for use in UNIX environments. The chip contains eight fully independent full-duplex UARTs and includes a host-system bus-interface controller that allows the chip to work in systems with bus speeds of up to 33 MHz and perform serial data transfers at rates of up to 16 Mbits/s. In addition, the UART chip includes two 16-bit multifunction programmable counters and a baud-rate generator, which creates 28 user-selectable baud rates. Other capabilities include programmable character recognition, a context-sensitive interrupt system and vectors, and automatic address detection. The chip operates from a 5-V supply, but may also be powered by 3.3 V to minimize power consumption. Available with either a Motorola- or Intel-style bus interface—the SC68C198 and SC26C198, respectively— the octal UART sells for $30 each in lots of 10,000. Both versions are now available with delivery from stock. CA

Philips Semiconductors, 811 E. Arques Ave., P.O. Box 3409, Sunnyvale, CA 94088-3409; Nitin Deo, (408) 991-4870. **CIRCLE 681**

256-KBIT SRAM FOR LOW-POWER SYSTEMS

The HM62W256, a CMOS static RAM, has been optimized for use in cache and buffer memories in hard-disk drives as well as in portable battery-powered computer applications. Offering an access time of 70 ns, the SRAM operates from a 3.3-V supply and consumes just 0.66 µW during standby. Organized as 32 kwords by 8 bits, the static RAM requires no clocks or timing strobes for operation. The HM62W256 comes in either a 26-pin small-outline J-lead (SOJ) package or a 32-pin thin small-outline package. Samples of the SOJ version are available from stock. In lots of 1000 units, it sells for $6.25 each. CA

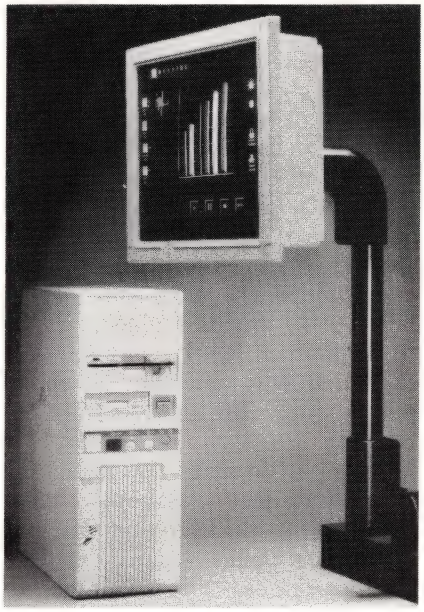
Hitachi America, Ltd., Semiconductor and I.C. Division, Hitachi Plaza, 2000 Sierra Point Parkway, Brisbane, CA 94005-1819; (415) 583-4207. **CIRCLE 682**

FAST 22V10 PAL DEVICE CLOCKS IN AT 142 MHZ

The PALCE22V10H-5, the latest member of a reprogrammable 5-ns PAL family from Advanced Micro Devices, is one of the fastest 221V0's currently available. Manufactured with the company's low-power electrically erasable EECMOS technology, it has a maximum clock frequency of 142.8 MHz and can be used in systems employing the fastest microprocessors. The parts varied product term distribution permits configuration of up to 16 product terms per output for complex functions. The PALCE22V10H-5 is available now in a 28-pin PLCC package. In lots of 1000 units, the chip sells for $27.50 each. CA

Advanced Micro Devices Inc., 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088-3453; (408) 749-5703. **CIRCLE 683**

TOUCH-SCREEN TERMINALS HOLD FLAT-PANEL VGA DISPLAYS



Rugged flat-panel VGA monitors now fit into the ErgoTouch family of computer-based touch-screen terminals. The user-configurable systems offer a small footprint package that can withstand repeated use in a harsh environment. The monitor, which is about 70% smaller and lighter than CRT-based displays, supplies the user interface. The complete package is sealed on all sides so it doesn't require an extra enclosure for operation.

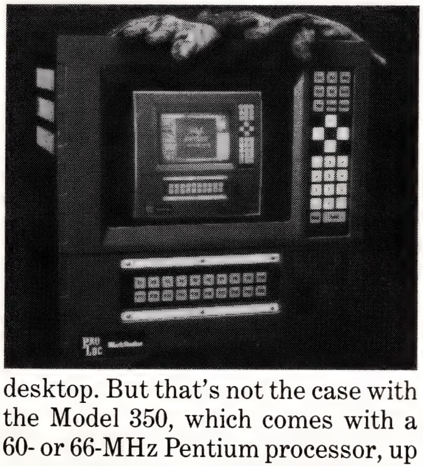
Three different configurations are available. The ErgoTouch Computer lets developers devise applications using standard PC tools. The applications are then downloaded to the system for use as a standalone or networked device. Systems based on a 386 microprocessor are available now. Upgrades to a 486 CPU are being readied. Many mass-storage and interface options are available. The ErgoTouch Monitor is a flat-panel VGA monitor and the ErgoTouch Terminal is a smart terminal that's compatible with ANSI character-based terminals and also incorporates PC technology. Prices for the computer range from $2950 to $9900.

Dynapro Technologies Inc., *800 Carleton Ct., Annacis Island, New Westminster, B.C., Canada V3M 6L3; (800) 667-0374 or (604) 521-3962.* CIRCLE 684

■ *RICHARD NASS*

INDUSTRIAL PLATFORM HOLDS PENTIUM CPU

Pentium-based PCs are starting to hit the mainstream on the desktop, but not in industrial workstations, whose technology typically lags the desktop. But that's not the case with the Model 350, which comes with a 60- or 66-MHz Pentium processor, up to 32 Mbytes of 64-bit RAM, 256 kbytes of cache memory, and local-bus video. The workstation's front panel is NEMA rated, and includes an impact- and scratch-resistant shield and an optional touch screen. The system has space for 18 I/O boards in its passive backplane. It is specified for up to 15 Gs of shock, 0.006-in. peak-to-peak vibration, and 0 to +55°C temperatures. The Model 350 industrial workstation sells for under $11,000. RN



Pro-Log Corp., 2555 Garden Rd., Monterey, CA 93940; (800) 538-9570 or (408) 372-4593. CIRCLE 685

COMMUICATION DEVICES FIT PCMCIA TYPE II SLOTS

Two products, each based on the PCMCIA standard, let users communicate while using portable PCs. The M144PA is a 14.4-kbit/s fax-modem that adheres to all relevant industry standards. The BEN1PA is a 10Base-T Ethernet adapter that connects to IEEE-standard 802.3 networks. Both communications-based cards fit the Type II PCMCIA form factor (5 mm high).

The M144PA automatically detects and handles incoming data calls and offers such features as auto dial and answer, tone or pulse dialing, and the ability to store configuration information in non-volatile memory. A fax can be received under Windows, whether the accompanying software is running in the foreground or background. Transmissions can be sent to either a single receiver or broadcast to a group. Available now, the M144PA PCMCIA-based fax modem costs $369. The BEN1PA, which sells for $229, has an operating distance of 100 meters and includes a 10Base-T twisted-pair transceiver with an RJ-45 connector. Drivers are included with both cards to support most major networking operating systems. RN

Boca Research Inc., 6413 Congress Ave., Boca Raton, FL 33487; (407) 997-6227. CIRCLE 686

16-BIT AUDIO FUNCTIONS FIT IN PCMCIA CARD

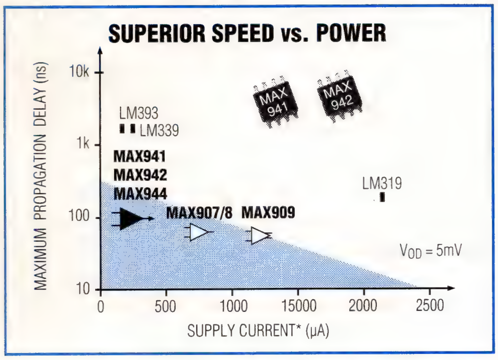
A 16-bit stereo sound card, bundled with Microsoft's Windows Sound System software and a series of plug-and-play drivers, all fit in to a Type 1 PCMCIA card. Designed for presentation audio, multimedia applications, and voice navigation, the .WAVjammer supplies a complete sound solution for users of portable systems or any other system containing a PCMCIA slot. The card can record and play back 16-bit stereo sounds with sampling rates reaching 44.1 kHz. It also supplies advanced 20-voice synthesis.

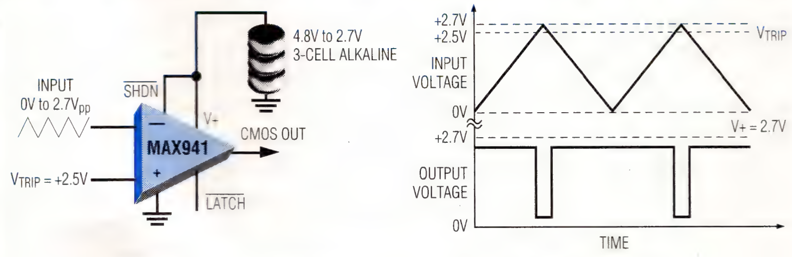
Using DMA emulation, large blocks of data can be buffered, allowing the card to operate with less than 2% of the CPU bandwidth. Weighing in at 7 oz., the card connects to peripherals through a thin 6-in. cable, which holds stereo jacks for a headset, a microphone, and input and output lines. The integrated software gets users up and running quickly. The .WAVjammer is available now for $399. RN

New Media Corp., Irvine Spectrum, 15375 Barranca Pkwy., Building B101, Irvine, CA 92718; (714) 453-0100. CIRCLE 687

INDUSTRY'S FIRST RAIL-TO-RAIL, 100ns COMPARATORS OPERATE DOWN TO 2.7V!

Input Range Extends Beyond the Supply Rails, Only 350µA Supply Current





With inputs that extend **beyond** the supplies, these devices compare signals as large as the supply without power-consuming resistor dividers.

- Single & Dual in 8-pin SO
- Quad in 14-pin SO
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- No External Pull-Ups Required

The new MAX941 single, MAX942 dual, and MAX944 quad are the first high-speed, low-power comparators guaranteed to operate from a 2.7V single-supply with a propagation delay of less than 100ns. And to simplify 3V and 5V designs even further, inputs extend **beyond** both supply rails, and outputs are CMOS/TTL compatible without external pull-ups.

Select the Ideal 3V or 5V High-Speed Comparator From the Industry Leader

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NEW MAX941†	Single	100	350 12(SHDN)	2.7V	-200mV to 5.2V	$1.40
NEW MAX942	Dual	100	350	2.7V	-200mV to 5.2V	$1.50
NEW MAX944	Quad	100	350	2.7V	-200mV to 5.2V	$2.50
MAX907	Dual	50	700	5V	-200mV to 3.5V	$1.70
MAX908	Quad	50	700	5V	-200mV to 3.5V	$2.95
MAX909	Single	50	1200††	5V	-200mV to 3.5V	$1.50

*Supply Current is per comparator, T_A = 25°C
**1000-up recommended resale, FOB USA
†MAX941 available in April, 1994.
††MAX909 has complementary outputs

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READER SERVICE 169

FPGA TOOLS SUPPORT 0.5-μM TECHNOLOGY

New features in AT&T's Orca Development System (ODS) software support the company's 0.5-μm high-density devices. ODS Version 2.0 supports all existing devices in the Orca FPGA family as well as the 0.5-μm 12,000- and 15,000-gate parts. New features include back-annotated timing for post-routing simulation to the original schematic, net-list merge, algorithm improvements for datapath-intensive designs, and an enhanced design editor with incremental logic change capabilities. Design entry is performed with third-party tools, such as those from Viewlogic and Exemplar. ODS 2.0 runs on Sun workstations, and under Windows on PCs. The software is shipping now. Pricing is set at $4500 and $7500 for the PC and Sun versions, respectively. LM

AT&T Microelectronics, 555 Union Blvd., Allentown, PA 18103; (215) 439-6011. **CIRCLE 688**

BACKPLANE FACILITATES MIXED-LEVEL SIMULATION

The Vertue simulation backplane from Epic Design Technology meshes the company's TimeMill and PowerMill timing and power simulation tools with the Verilog-XL simulator. The TimeMill and PowerMill tools perform transistor-level simulation. Vertue features automatic net-list splitting and simulation control from any of the tools. In addition, it enable hierarchical design of deep submicron silicon. Engineers start with register-transfer or gate-level descriptions, and switch to the transistor level on a block-by-block basis. The transistor-level simulation yields Spice-like accuracy, and ensures that engineers catch all the subtle problems that are invisible at the gate level. Then, the engineers can characterize the block, and trade back to the register-transfer level. Vertue is supported on Sun Sparcstations running Verilog-XL versions 1.6a4, 1.6a7, and 1.6b. Pricing for a node-locked, single-user license is $18,000. LM

Epic Design Technology Inc., Suite 212, 2901 Tasman Dr., Sanata Clara, CA 95054; (408) 988-2997. **CIRCLE 689**

SOFTWARE AUTOMATES LIBRARY DEVELOPMENT

ASIC and custom-IC library-generation software helps users get up and running on the Zycad simulation accelerators within days instead of the months of preparation that were previously required. The Paradigm Library Toolset automates the development of Zycad XP and Paradigm XP libraries from a standard ASIC library format (Verilog source libraries). The toolset consists of three software packages: the VeriFE Verilog-to-Zycad format translator, the Libertee library compiler, and the Certifi library verifier. VeriFE translates gate-level Verilog source libraries into a Zycad intermediate format. The Libertee library compiler then generates Zycad-specific EDIF libraries. Paradigm Library Toolset runs on workstations. The translator costs $15,000, and the library compiler and verifier are bundled together for $15,000. LM

Zycad Corp., 47100 Bayside Pkwy., Fremont, CA 94538-9942; (800) 243-7286. **CIRCLE 690**

VHDL SIMULATORS MEET VARYING GROUP NEEDS

The first two products in a new VHDL System Simulator (VSS) family from Synopsys enable design work groups to select the optimal mix of simulation capacity to match their design flow and budget. The first product, VSS Professional, is tailored for individual use during pre-synthesis VHDL model development and system verification. It combines interpreted and compiled simulation engines, which are tightly integrated through one simulation time wheel. The other product, called VSS Expert, includes all of the VSS Professional features plus a specialized gate-level sign-off simulation engine, system-level modeling support, and ASIC vendor sign-off support. Because the simulators are tightly meshed, design groups can choose the best simulation technology for each phase of design. VSS Professional and VSS Expert run on Unix workstations, and cost $13,000 and $24,000, respectively. LM

Synopsys Inc., 700 E. Middlefield Rd., Mountain View, CA 94043-4033; (415) 962-5000. **CIRCLE 691**

FPGA LAYOUT SYSTEM LINKS WITH SYNTHESIS

Release 4.1 of the FPGA Foundry device-independent design tools features a timing interface to synthesis software called Top-Down Design Link. FPGA Foundry is an FPGA back-end design environment that supports multiple vendors and architectures, integrates into existing CAE environments, and provides timing-and frequency-driven design. Top-Down Design Link automatically interprets, configures, and passes the timing constraints that are specified during logic synthesis to the FPGA tools for timing- and frequency-driven implementation. This enables users to accurately predict and control device timing through the FPGA design process. In addition, Release 4.1 introduces support for Motorola's MPA1036 device family, a new version of a multichip partitioning module, an enhanced LPM library, and a design interface with Logic Modeling's SmartModels. Pricing for the Motorola system, Top-Down Design Link, and the partitioning module starts at $3995, $2500, and $3995, respectively. LM

NeoCAD Inc., 2585 Central Ave., Boulder, CO 80301; (303) 442-9121. **CIRCLE 692**

TRANSLATE STATE DIAGRAMS INTO ABEL

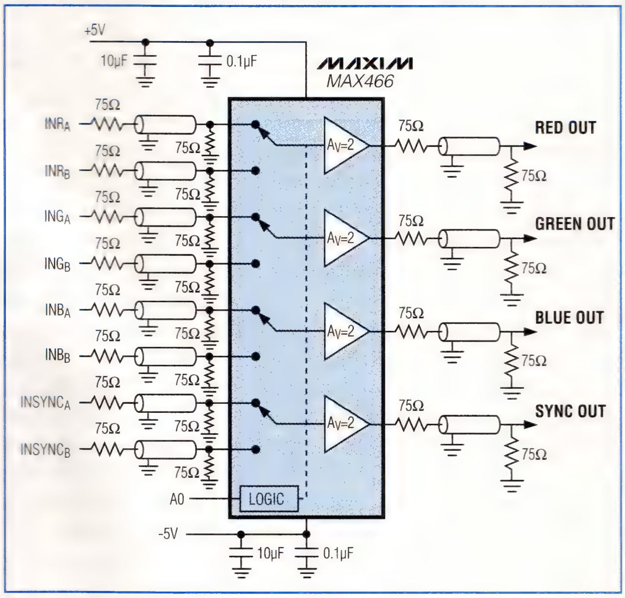
A Windows-based design-entry tool called StateCAD generates synthesizable ABEL descriptions from state diagrams. The software includes a drawing engine tailored to the rendering of state diagrams, as well as a context-sensitive validation unit that flags syntax and logic errors. StateCAD creates ABEL hardware-description-language files that are fed directly into an ABEL compiler for simulation or device programming. In addition, the generated HDL file can be either architecture dependent or independent. StateCAD supports a variety of logic-entry methods, including Mealy/Moore machines and complex array operations. The StateCAD software, which runs on PCs, is shipping now for $995. LM

Visual Software Solutions Inc., 3057 Coral Springs Dr., Suite 203, Coral Springs, FL 33065; (800) 208-1051. **CIRCLE 710**

100MHz RGB VIDEO SWITCHES INCLUDE 75Ω OUTPUT DRIVERS

Switch Between Two RGB Channels in 20ns, Directly Drive ±2.0V into 75Ω

- **100MHz Bandwidth**
  MAX463/MAX464 (A_V = 1V/V)
- **90MHz Bandwidth**
  MAX465/MAX466 (A_V = 2V/V)
- **300V/µs Slew Rate**
- **Hi-Z Output State**
- **5pF Input Capacitance**
- **±2.5V Output Swing Into 150Ω**



The MAX463-MAX466 are four new ±5V video ICs that switch between two RGB or RGB + Sync channels **and** include 100MHz output drivers. For design flexibility, the triple (RGB) or quad (RGB + Sync) versions are available with either unity-gain or fixed gain-of-two drivers for driving back-terminated coaxial cable. In addition, a high-impedance disable mode reduces supply current and allows multiple switches to be paralleled in larger networks.

Simplify Video Routing with Maxim's New RGB Switches

DEVICE	DESCRIPTION	VOLTAGE GAIN (V/V)	BANDWIDTH (MHz)	SLEW RATE (V/µs)	MINIMUM OUTPUT SWING (R_L = 75Ω)	Hi-Z OUTPUT STATE
MAX463	2-Channel RGB Switch with Output Drivers	1	100	200	±2.0V	YES
MAX464	2-Channel RGB + Sync Switch with Output Drivers	1	100	200	±2.0V	YES
MAX465	2-Channel RGB Switch with Output Drivers	2	90	300	±2.0V	YES
MAX466	2-Channel RGB + Sync Switch with Output Drivers	2	90	300	±2.0V	YES

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READER SERVICE 194

GSM TEST SOFTWARE ADDS LOAD-TRAFFIC SIMULATION

Software release 5.3 of the Global System for Mobile communications Tester (GSM-T) features the ability to generate load traffic on the C and D interfaces to verify the operation and performance of Home Location Registers (HLRs). GSM is the European digital mobile phone standard. The tool performs load testing of key network devices in the GSM's network infrastructure.

The software enables system developers, software suppliers, and the operational service centers of wireless-network operators to simulate realistic call-traffic load conditions via the C and D interfaces to verify the roaming capability of networks. Load testing of the C and D interfaces helps switch manufacturers improve the performance of their HLRs by identifying call-capacity issues.

The software's new features include treatment of mobile subscriber roaming (involving the handover of calls among GSM network devices), enhanced message buffering (for example, a hot key that enables quick display of messages by call transaction), and a ten-fold expansion of database capacity (more storage for mobile subscriber data). Other features are a three-fold expansion in the size and number of load test scripts per link (enabling the generation of a more powerful load traffic mix), and a reduction in the time required to initialize data in the GSM-T links (from minutes to seconds).

The capability of the GSM-T to generate load on the voice link (TRAU) of the Abis interface is in beta testing and scheduled for release in the first quarter of 1994. Load generation of the Short Message Service (SMS) and Supplementary Services (SS) procedures, also in beta testing, is expected to be released around the same time.

Components of the GSM-T include an Administrative System (UNIX workstation); 19- or 23-in. shelves (hardware systems that perform passive and/or active diagnostics); and software applications for simulation, emulation, load testing, and monitoring. Pricing for a GSM-T starts at $55,000.

Tekelec, *26580 West Agoura Rd., Calabasas, California, 91302; (818) 880-5656; fax (818) 880-6993* **CIRCLE 693**

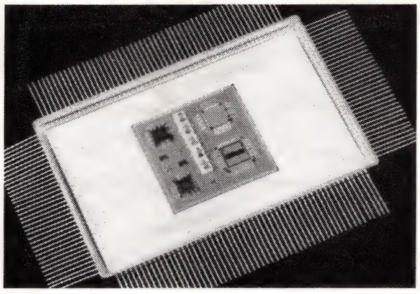
■ *CLIFFORD METH*

622-MBITS/S ATM CHIP SET INCLUDES MCM IMPLEMENTATION

A new chip set is designed to implement physical layer interfaces for asynchronous-transfer-mode (ATM) applications operating at 622 Mbits/s. The chip set, from PMC-Sierra, Burnaby, Canada, uses SONET and SDH transmission standards and has uses in ATM backbones, campus networks, public-network access and carrier-transmission systems.

Within the set are three chips and one multichip module: the PM5312 STTX SONET/SDH transport-terminating transceiver, the PM5318 SIPO serial-parallel conversion chip, the PM5345 Saturn user-network (SUNI) interface chip, and the PM5712B SLIM SONET/SDH line-interface multichip module.

The PM5345 SUNI chip incorporates modes for use in either standalone 155-Mbit applications, or in the 622-Mbit application. The SUNI processes 155-Mbit/s ATM streams and connects directly to the PM5312 STTX chip, which provides byte-interleaved multiplexing and transport overhead processing of up to four individual streams. The STTX device, in turn, connects to the PM5318 SIPO chip, which converts the 78-Mbyte/s byte streams from the STTX into bit-serial 622-Mbit/s ECL-compatible signals. These signals then connect directly with optical-fiber interface and clock-recovery modules to implement a SONET or SDH-compliant interface.



In the multichip-module implementation of PMC's existing PM5712 SLIM product, users will find enhanced operation. The PM5712B SLIM contains the SIPO and STTX chips and integrates clock recovery and clock synthesis onto one metal quad-flat-pack module. The PM5712B provides additional features for SONET and SDH compliance, lower operating power, and a lower cost than its original version. The PM5712B will find use in applications where users want a complete 622-Mbit/s interface, including clock recovery and generation contained in one shielded package, or in situations where board space is tight.

The chip set maps ATM cell streams from an ATM switch core onto a 622-Mbit/s serial data stream. Four SUNI chips connect to the switch core on one side and provide FIFO buffering and ATM cell mapping into a SONET/SDH 155-Mbit stream. Using the SUNI parallel-line side port, the four SONET/SDH ATM streams from the SUNI chips then connect directly to the PM5312 STTX chip.

The PM5312 STTX chip is available in a 208-pin, copper-slugged plastic quad flat pack (PQFP) for $170 in lots of 10,000. The PM5318 SIPO chip comes in a 128-pin, copper-slugged PQFP and costs $120 in similar quantites. The PM5712B SLIM module comes in a 182-pin Kovar flat pack for $1100 in similar quantities. The PM5345 SUNI-155 chip comes a 160-pin PQFP and costs $47.60 in lots of 100,000. All are available now in sample quantities.

PMC-Sierra Inc., *8501 Commerce Ct., Burnaby, British Columbia, Canada, V5A 4N3; Vernon Little, (604) 668-7348.* **CIRCLE 694**

■ *CLIFFORD METH*

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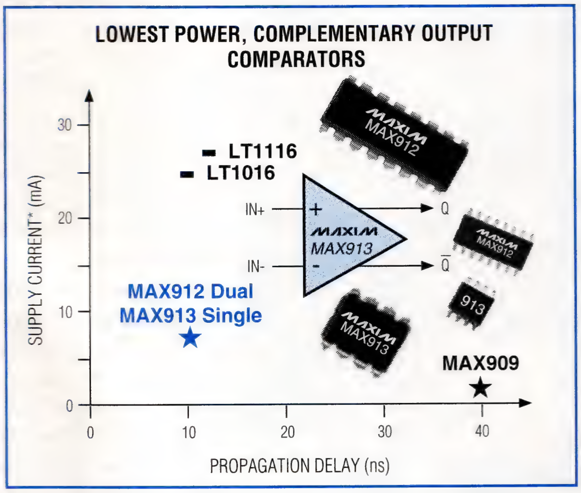

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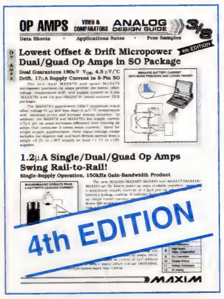
	COMPARATORS PER PKG	PROP DELAY (ns)	SUPPLY CURRENT* (mA)	INPUT VOLTAGE RANGE (V+ = 5V, V- = GND)	COMPLEMENTARY OUTPUTS
MAX912	**Dual**	**10**	**7**	**GND to 3.5V**	**YES**
MAX913	**Single**				
LT1016	Single	10	25	1.25V to 3.5V	YES
LT1116	Single	12	27	GND to 2.5V	YES
MAX901	Quad	8	2.5	GND to 2.75V	NO
MAX902	Dual				
MAX903	Single				
MAX907	Dual	40	0.7	GND to 3.5V	NO
MAX908	Quad				
MAX909	Single	40	1.2	GND to 3.5V	YES

*Positive Supply Current per Comparator; V+ = 5V, V- = GND.



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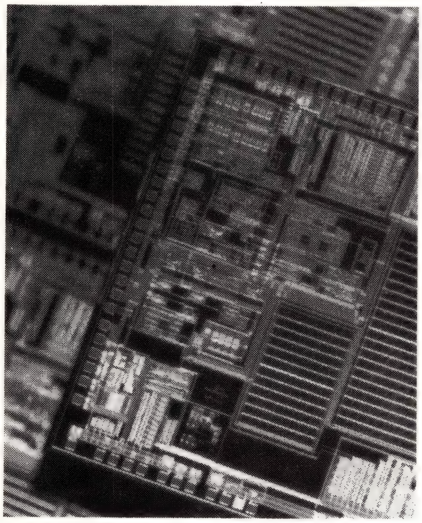
READER SERVICE 195

TRANSMIT/RECEIVE CHIPS SIMPLIFY FAST LINKS

For designers of high-speed serial interfaces, the RCC700 and 701 fully integrated transmitter/receiver chips reduce the task's complexity. The chips run at the 265.625-Mbaud data rates of Fibre Channel, the 200-Mbaud rates for ESCON (enterprise systems connection architecture) and SSA (serial storage architecture), and the 194.4-Mbaud rate for ATM (asynchronous transfer mode).



The CMOS RCC700 transceiver incorporates an 8B/10B encoder/decoder, a serializer/deserializer, a phase-locked-loop-based frequency synthesizer, a PLL-based clock-and-data-recovery block, and byte-alignment circuitry, all in a 68-lead PLCC or 64-lead PQFP. If the 8B/10B encoder and decoder functions aren't needed, the RCC701 provides all the other functionality with a 10-bit interface so the host system can perform its own encoding/decoding scheme. Serial data moves over the interface using positive-referenced ECL levels.

At 200 Mbaud and powered by a 5-V supply, the RCC700 consumes about 600 mW; the 701 draws about 550 mW. In lots of 10,000, the plastic leaded chip-carrier version of the RCC700 sells for $32.10 each; the RCC701 costs $29.90 each. Samples are immediately available from stock. DB

Raytheon Co., Semiconductor Div., 350 Ellis Street, P.O. Box 7016, Mountain View, CA 94039-7016; Jack Guedj, (415) 968-9211. CIRCLE 695

SPREAD-SPECTRUM IC AND I/O STAGE SMOOTH WIRELESS-PHONE DESIGN

Providing access to hundreds of clear channels, up to four hours of continuous talk time, 18 hours of standby time, and many other features, the WLT-9009 spread-spectrum chip and complementary 900-MHz RF I/O-stage design simplify the development of inexpensive cordless telephones. Developed by Wireless Logic Technologies, the spread-spectrum chip also allows a choice of over 7 million security codes and includes automatic power-down control logic to minimize power drain. The chip delivers clear channels with no dead spots and, when used with the RF I/O stage design, can transmit up to 5 miles with a 100-mW power output.

On the WLT-9009 is a DSP core, mixed-signal circuits to handle the voice signals, and direct-sequence spread-spectrum communications circuitry and algorithms. The spread-spectrum chip implements direct-sequence spread-spectrum communications, in which signals are multiplied with a pseudo-random noise or phase-modulation code, the result of which can be distributed "evenly" over the entire band.

To implement a full wireless phone, the WTL-9009 must be surrounded by a microcontroller, an rf I/O stage, a keypad, some display indicators, and some other components. The Spread Spectrum chip operates from a 5-V supply and consumes about 20 mA when active, and about 3 mA when idling. Housed in a 64-lead PQFP, the WLT-9009 sells for about $15 in OEM quantities. Samples are available now.

Wireless Logic Technologies Ltd., *4010 Moorpark Ave., Ste. 105F, San Jose, CA 95117; James Wong, (408) 246-1538.* CIRCLE 696

■ *DAVE BURSKY*

COMPACT OPTICAL TRANSCEIVER HANDLES GIGABIT DATA RATES

Available as either a combination optical transmitter and receiver, or as separately packaged transmit and receive modules, the FTM-8510 series of gigabit optical interfaces gives designers a choice of compact formats. The transceiver module is an integrated version of three of Finisar's previously released products: the FTM-8500 transmitter, the FTR-8500 receiver, and the FCC-2000 link controller. The FTM-8510 can deliver optical data streams at 100 Mbits/s to 1.5 Gbits/s based on the company's proprietary short-wavelength multimode optics scheme.

The all-in-one FTM-8510 module, which measures just 1.5-by-2-by-0.4 in., reduces board space, power consumption, and component height by more than 25%, when compared with the company's previous offering. In addition, the module runs from a 5-V supply; the previous solution required both 5- and 12-V supplies.

Inside the module, the custom link-controller chip (which in the first iteration of the module) implements the open-fiber control-protocol, which is specified by the Fibre Channel Standards Association (ANSI X3T9.3). The wide data-rate range makes it possible for the module to handle all of the Fibre-Channel rates from 133 to 1062 Mbits/s, as well as ATM transfers at 155 to 1244 Mbits/s and the HiPPI serial and scalable coherent interfaces.

In small quantities (10 or less), the FTR-8510 sells for $660 each. Samples are available from stock. In pairs, the separate receive and transmit interface modules will also cost about $660. Long-wavelength lasers, which can go over large cable distances, are also available: One transceiver pair costs about $1600.

Finisar Corp., *3515 Edison Way, Menlo Park, CA 94025; Jerry Rawls, (415) 364-2722.* CIRCLE 697

■ *DAVE BURSKY*

TOOL GENERATES CODE FRAMES FROM OOA MODELS

SES/objectbench Frame Builder, a computer-aided software engineering (CASE) tool, automates coding tasks that would otherwise have to be done manually. Frame Builder generates C++ code frames directly from Shlaer-Mellor object-oriented analysis (OOA) models. The output comprises two files: one containing class declarations and the other containing implementation details, such as constructors, destructors, public functions, key methods, and private methods.

FrameBuilder is the third member of the SES/objectbench product family. Other tools include a graphical modeler for building models and an animated simulator for testing and verifying model execution. The Shlaer-Mellor method is developed and supported by Project Technology, Berkeley, Calif.

With the graphical model, users can quickly and accurately develop information models, state models, and process models. A graphical, menu-driven interface, with editing features and multilevel semantic checking, automates building OOA models.

The animated simulator automates the testing process for OOA models. Using a VCR-like interface and on-screen animation, users control the behavior of Shlaer-Mellor models and run frequent, interactive testings. Debugging features, such as breakpoints and rules-based conditional breaks, give the user a fine degree of control over execution behavior. By using simulation, the user can confirm proper model execution before coding begins. Frame Builder, which runs on Sun, HP, and IBM workstations, starts at $5900.

Scientific and Engineering Software Inc. (SES), *4301 Westbank Dr., Building A, Austin, Texas 78746-6564; (512) 328-5544; fax 327-6646.* **CIRCLE 698**

■ *SHERRIE VAN TYLE*

DSP SOFTWARE PLATFORM TARGETS MULTIMEDIA

A software platform for PCs with digital signal processors is based on the SPOX real-time multitasking DSP operating system. The DSP-resident SPOX Multimedia Platform works with Microsoft's SPOX-based DSP applications programming interface (API), also known as the Resource Manager Interface, which runs under Windows on the PC host. The platform targets multimedia hardware original equipment manufacturers integrating digital signal processors to combine such functions as fax/modem, audio, video, and speech compression.

For hardware OEMs, having a standard real-time OS and API gives them access to a broad range of Windows applications and the flexibility to select DSPs from multiple vendors. For application developers, the availability of a DSP API gives them access to the computing resources for creating multimedia applications. The hardware-independent DSP API enables them to transparently access DSP ICs from several vendors—the platform supports designs based on processors from Texas Instruments, Analog Devices, and Motorola.

The SPOX real-time kernel, which interacts directly with the DSP, schedules multiple DSP tasks, synchronizes DSP tasks, and establishes communication between tasks using message queues, mailboxes, and semaphores. To simplify task development, the OS supplies a device-independent streaming I/O mechanism that enables a single DSP task to read/write data from multiple devices such as serial ports, ADCs, and telephones.

Development licenses for the SPOX Developer's Kit, which includes the SPOX real-time OS, SPOX monitor, multimedia device drivers, and a reference board support package, start at $15,000. Specifications for the Windows DSP software architecture will be available from Microsoft in the first half of this year.

Spectron Microsystems, *320 Storke Rd., Goleta, CA 93117; (805) 968-5100; -9770.* **CIRCLE 699**

■ *SHERRIE VAN TYLE*

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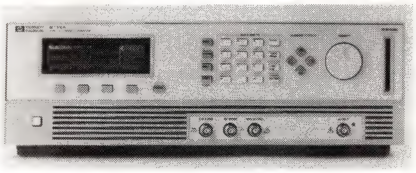
READER SERVICE 189

ETHERNET KIT LINKS MACS TO GPIB INSTRUMENTS

The GPIB-ENET/Mac is an external interface kit that uses Ethernet networks to connect Macintosh computers to IEEE-488 instruments or to other GPIB-ENET-equipped Macintosh computers, Sun Sparcstations, and Hewlett-Packard 9000 Series 700 workstations. The GPIB-ENET/Mac kit has an internal power supply and includes high-level NI-488.2 software, which has over 50 GPIB-related routines and functions that simplify programming. The kit requires a Macintosh host running MacTCP and access to a TCP/IP network. The interface is available immediately for $1095 for the twisted pair version, and $1195 for the coaxial version. Prices are for single-computer use. An optional software site license is also available. JN

National Instruments Corp., 6504 Bridge Point Pkwy., Austin, TX 78730-5039; (800) 433-3488 or (512) 794-0100. **CIRCLE 700**

PROGRAMMABLE UNIT OFFERS 100-V, 2-A PULSES



The HP 8114A programmable pulse generator targets the characterization and testing of high-voltage and current components at up to 15 MHz. The generator supplies variable duty-cycle pulses at up to 100 V or 2 A with 1% amplitude accuracy and 7-ns transition times. Timing resolution of 100 ps and amplitude resolution of 10 mV are available. To protect devices under test, the unit has adjustable level and duty-cycle limits and an inhibit-output feature that shuts down the output if a device shows signs of overload. An optional variable baseline capability eliminates the need for an external power supply by creating a ±25-V offset. The HP 8114A costs $9600, and the variable baseline option is $1700. Estimated delivery is in two weeks. JN

Hewlett-Packard Co., Direct Marketing Org., P.O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844 ext. 7961. **CIRCLE 701**

FAST TESTERS TARGET COMPLEX DEVICES

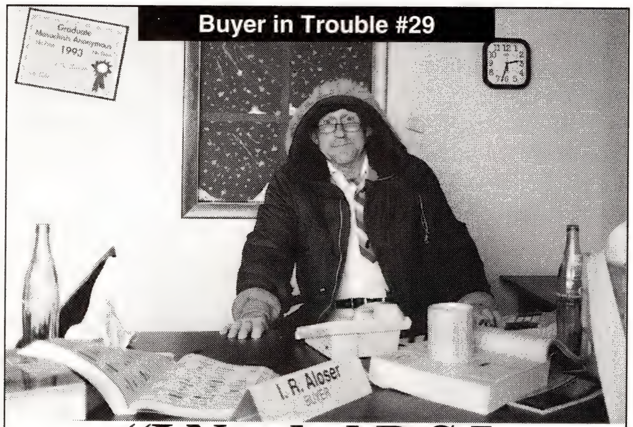
ATS Blazer! is the core-digital engine for a high-throughput test-station line optimized for the large volumes of information and multiple operations needed to debug and test complex devices. Systems available with ATS Blazer! include the MCM Test Station and wafer- and package-sorting stations. Maximum data rates are either 125 or 200 MHz, with full per-pin programmability and scan modules of up to 32 Mbits of serial memory per channel. It works with a wide variety of simulation environments and can be configured in 16-pin increments to 832 pins. Systems cost from $2500 to $3000 per pin, depending on the data rate. JN

Integrated Measurement Systems Inc., 9525 S.W. Gemini Dr., Beaverton, OR 97005; (503) 626-7117. **CIRCLE 702**

LOW-PRICED DSOs ELIMINATE ALIASING

The TDS 310 (50-MHz) and TDS 350 (200-MHz) real-time digital oscilloscopes feature a proprietary high-speed oversampling technique that eliminates the potential for aliasing of the waveform. The TDS 310 digitizes at 200 Msamples/s and the TDS 350 at 1 Gsample/s. The two-channel scopes have an intuitive user interface that captures the simplicity of an analog scope interface, and a fast update rate that creates a continuous display similar to that of an analog scope. Users can choose a dot or vector display. The units make over 20 waveform measurements and offer sample, envelope, average, and peak detect modes. An optional communications interface includes IEEE-488, RS-232, and Centronics ports. The TDS 310 costs $2295 and the TDS 350 costs $3995. JN

Tektronix Inc., Test and Measurement Group, P. O. Box 1520, Pittsfield, MA 01202; (800) 426-2200 ext. 201. **CIRCLE 703**



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READER SERVICE 122

LONG-MEMORY SCOPES BOAST FULL CONFIGURABILITY

The 9350-series digital oscilloscopes allow users to configure digitizers and memories to get up to 2-Gsample/s digitizing and 8 Mbytes of memory on one channel. All units have a state-of-the-art 8-bit, 500-Msample/s flash analog-to-digital converter for each channel. Bandwidth is 500 MHz.

The 9350 has two channels and the 9354 has four channels. Both instruments come in a base version with 25 kbytes of memory per channel, an M version with 100 kbytes per channel, and an L version with 2 Mbytes per channel. Unlike other digital scopes that allow users to combine channels for higher digitizing rates, the 9350 series also combines the channel memories so that the horizontal resolution and total capture time remain the same. As a result, the 9354L can supply 2-Gsample/s digitizing with an 8-Mbyte memory on one channel. The scope's high processing speed allows it to perform waveform math and processing, including fast Fourier transforms, on an entire 8-Mbyte record.

Often, the peak-detect circuit in high-end digital scopes has the undesirable effect of causing a severe loss of horizontal (time) precision. This happens because detected peaks are known to have occured during a certain interval, but the specific time at which they occur is not known. This may make the acquired signals unsuitable for further processing. The 9350-Series scopes solve this problem by maintaining both peak-detected and normally sampled waveforms for each signal.

The scopes come with IEEE-488 and RS-232 interfaces. A Centronics printer port is optional as are a DOS-compatible 3.5-in. and PCMCIA memory-card slot. In addition to edge and window triggering, the scopes' Smart Trigger capability includes glitch, pulse width, interval width, state- and edge-qualified dropout, TV, and pattern triggers. The four-channel scopes feature a five-input pattern trigger, and the two-channel scopes offer a three-input pattern. Basic waveform math and averaging are standard, with extended math and FFT capability optional.

The 9350 (50-kbyte memory) costs $9490, the 9350M (200 kbytes) costs $11,490, and the 9350L (4 Mbytes) costs $16,490. The 9354 (100 kbytes) costs $13,990, the 9354M (400 kbytes) costs $16,490, and the 9354L (8 Mbytes) costs $24,490. Delivery is in six weeks.

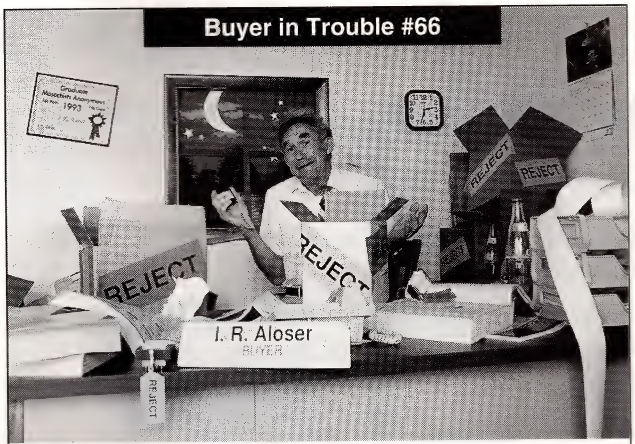
LeCroy Corp., *700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977-6499; (800) 453-2769.* **CIRCLE 704**

■ *JOHN NOVELLINO*

PACKAGE DOES ATPG FOR FULL- OR PARTIAL-SCAN

TestBench is an automatic test pattern generation tool for level-sensitive scan design (LSSD) and other scan methods used in full- or partial-scan circuits. Besides stuck-at and transition fault models, TestBench supports a new fault model called "pattern faults," which allow more accurate modeling of manufacturing defects like shorted nets. Pattern faults can be defined by TestBench users or by ASIC manufacturers. TestBench supports the industry-standard EDIF 2 0 0 input format, as well as formats produced by the IBM EDA LogicBench VHDL development environment. The software accommodates multiple output formats. TestBench runs on the IBM RS/6000 and PowerPCs running AIX, and the Sun Sparc and HP Series 700 workstations. Prices range from $50,000 for a system that handles up to 50,000 gates to $120,000 for a system that works with more than 250,000 gates. All include the graphical user interface. JN

Altium Corp., 1935 Buena Vista St., Burbank, CA 91504; (818) 841-9470. **CIRCLE 705**



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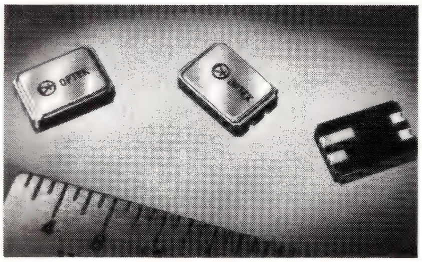
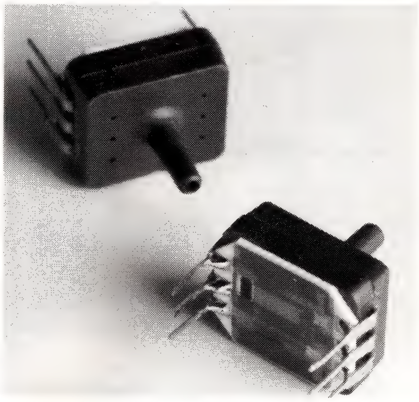


Optek Technology Inc., 1215 W. Crosby Rd., Carrollton, TX 75006; Andrew Kahn, (214) 323-2200. **CIRCLE 706**

DIP PRESSURE SENSORS HAVE STABLE OUTPUT

A solid cost-to-performance ratio in a convenient DIP configuration is offered by the SDX Series solid-state pressure sensors. The temperature-compensated devices meet requirements for calibrated span and offset from zero to 50°C, high stability and reliability, automated pc-board mounting, and low cost. Devices are available in absolute and gage configurations from 1 psi full scale to 100 psi. Output is ratiometric to the supply voltage, which can be from any dc source up to 20 V. Pricing is $16.10 in lots of 100. Small quantities are delivered from stock. DM



SenSym Inc., 1804 McCarthy Blvd., Milpitas, CA 95035; Fred Jones, (408) 954-1100. **CIRCLE 707**

TEMPERATURE PROBES MEET APPLIANCE NEEDS

A line of NTC thermistor probe assemblies is available for appliance applications. Incorporating Fenwal's NTC glass-encapsulated chip thermistors or R-T-curve-matched NTC Uni-Curve thermistors, the probe assemblies support and accurately locate the thermistor elements within the medium to be monitored. The assemblies also protect the thermistor against damage in use and handling. They fulfill temperature-sensing needs in a wide range of appliances such as microwave ovens, washing machines, clothes dryers, conventional ovens, air conditioners, and refrigerators. Pricing begins at less than $1 depending on type of assembly and unit quantities. Delivery is in eight to 10 weeks. DM

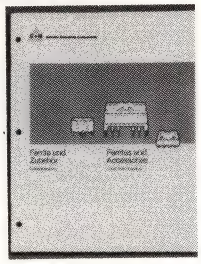
Fenwal Electronics Inc., 450 Fortune Blvd., Milford, MA 01757-1745; (508) 478-6000. **CIRCLE 708**

CUSTOM MEMBRANES OFFER FLEXIBILITY

Designed to accommodate custom membrane-switching applications, the Series 70 switches offer the end user a great deal of flexibility. The system features a drop-in metal-frame panel that can be customized to an engineer's specifications. The panel is available complete with mounted switches, pc-board connectors, and other components required for the application. For even more flexibility, the distance between the back of the front panel and the pc board is variable from 9 to 22.5 mm, allowing for addition of multiple components. The system also boasts a switching element with a lifespan of 5 million operations and available full-screen LED illumination with changeable embossed legends. Pricing averages $8 to $10 per function. Delivery is in 10 to 12 weeks. DM

EAO Switch Corp., 198 Pepe's Farm Rd., Milford, CT 06460; (203) 877-4577. **CIRCLE 709**

SHORT-FORM CATALOG FEATURES FERRITES



A comprehensive line of ferrites and accessories is featured in a 40-page short-form catalog from the Special Products Div. of Siemens Corp., Iselin, N.J. Information is included on low-profile versions of all RM cores, as well as many additions to the range of E/U cores. Also covered are new materials such as type N62, which offers initial permeability of $\mu_i = 1900$. This is suitable for frequencies up to 150 kHz and a large dc-biasing range. Photos, dimensional information, and electrical specifications are provided. DM **CIRCLE 930**

AXIAL-LEAD RESISTORS RATE REFERENCE GUIDE

A comprehensive listing of a full line of axial-leaded resistor products is featured in an eight-page reference guide from Ohmite Mfg. Co., Skokie, Ill. An easy-to-use cost-consideration guide categorized products by wattage rating and performance characteristics. A specifying cross-reference table gives users an identification tool for selecting the right resistor for their application. Detailed specifications for each series include material and electrical data, resistance ranges and tolerances, and complete dimensional drawings. DM **CIRCLE 931**

POWER NEWSLETTER COVERS COMM SUPPORT

The latest issue of a newsletter from Kepco, Flushing, N.Y., provides a compendium of information about power supplies. Volume 4, No. 2 of *Kepco Currents* offers stories on communication buses to control programmable power supplies, an announcement of Kepco's support for the VXI standard, a reprint of an article on fault-tolerant supplies, and a look back into the early days of the power-supply business. DM **CIRCLE 932**

POWER-SEMI GUIDE AIDS IN SELECTION

A product-selector guide showcases a broad line of discrete and modular power MOSFETs, IGBTs, fast-recovery epitaxial diodes (FREDs), thyristors, and rectifiers from IXYS Corp, Santa Clara, Calif. The 40-page guide includes over 100 new product types, each with a short description, a listing of the device's key performance characteristics, and package outlines. New devices span ultrafast-switching IGBTs, intelligent IBGT modules, power-factor-correction modules, and power MOSFETs with ultra-low on-resistance figures. DM **CIRCLE 933**

IN-STOCK CATALOG DETAILS TIMERS

A 32-page catalog of popular and in-stock control devices from SSAC Inc., Baldwinsville, N.Y., includes time-delay relays, encapsulated timing modules, universal timers, alternating relays, three-phase voltage monitors, current sensors, liquid-level controls, flashers, and accessories. A complete index and product-selection guide makes choosing the right device for a given application easy. Each page contains all the specifications needed to select one of the stock part numbers shown on that page. DM **CIRCLE 934**

ADAPTER CATALOG OFFERS DESIGN AIDS

Quick, easy location of the right adapters and accessories for a design-under-test is the point of the 1994 VLSI and SMT interconnect-solutions catalog from Emulation Technology Inc., Santa Clara, Calif. The 184-page tome can be used as a reference guide to a wide range of IC packages and chip types. More than 100 photos are included with data on over 3500 products including emulation tools, logic-analyzer/scope adapters, programming adapters, production/test adapters, debugging accessories, prototyping adapters, field-configurable adapters, and custom types. DM **CIRCLE 935**

THIN-FILM PRODUCTS FILL FULL-LINE GUIDE

Complete specifications are furnished in detail for an extensive line of precision resistor, capacitor, inductor, and diode combination networks in a variety of packages. The full-line, 120-page catalog from California Micro Devices, Milpitas, Calif., also includes a line of flip chips as well as application notes on EMI/RFI filtering and ac terminations. Dimensional diagrams are supplied for all devices as are tables of standard values and electrical characteristics. DM **CIRCLE 936**

SELECTOR OUTLINES INDUCTIVE COMPONENTS

A 24-page comprehensive guide to inductive components features a wide selection of standard products. The guide includes domestic power transformers for personal computers, an international series of transformers, telecommunication magnetics, inductors, and CRT-display magnetics. The brochure, from Prem Magnetics Inc., McHenry, Ill., offers full specifications and descriptions for all products. In addition, there is a convenient quotation-request form for custom designs. Information is included on agency approvals. Standard devices can be modified to meet any specifications or special needs. DM **CIRCLE 937**

DICTIONARY LISTS FIBER-OPTIC TERMS

A comprehensive 62-page dictionary of terms and definitions for fiber-optic communications is available from the Fiber Optic Div. of Methode Electronics Inc., Chicago. Well illustrated with drawings, the pocket-sized dictionary serves as a quick reference for users involved in fiber optics. Typical terms and definitions include acceptance angle, angular misalignment loss, bit rate, chromatic dispersion, diameter-mismatch loss, Fresnel reflection, loose-tube buffering, quantum efficiency, and Zirconium arc. Over 450 definitions are included. DM **CIRCLE 938**

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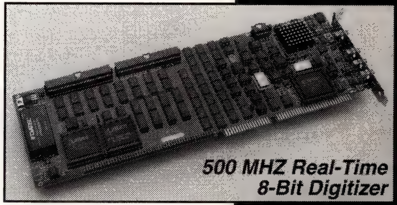

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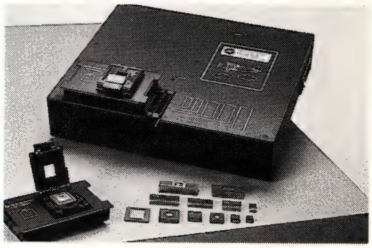

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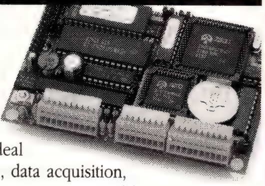

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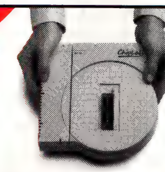

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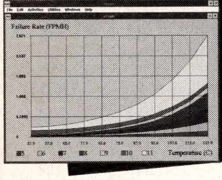

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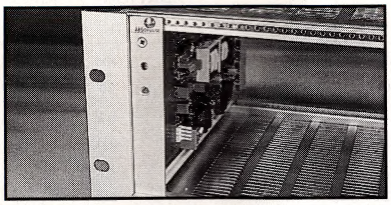

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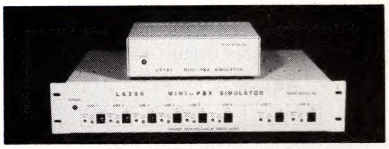

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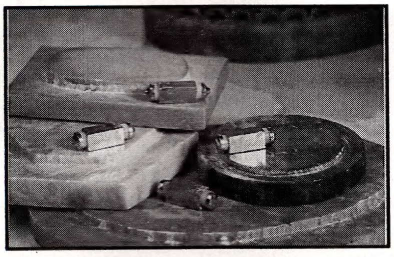

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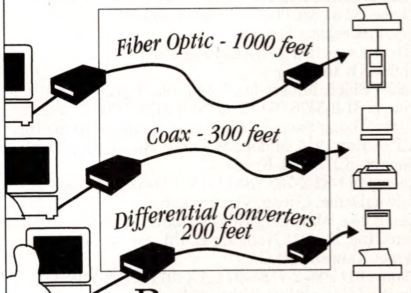

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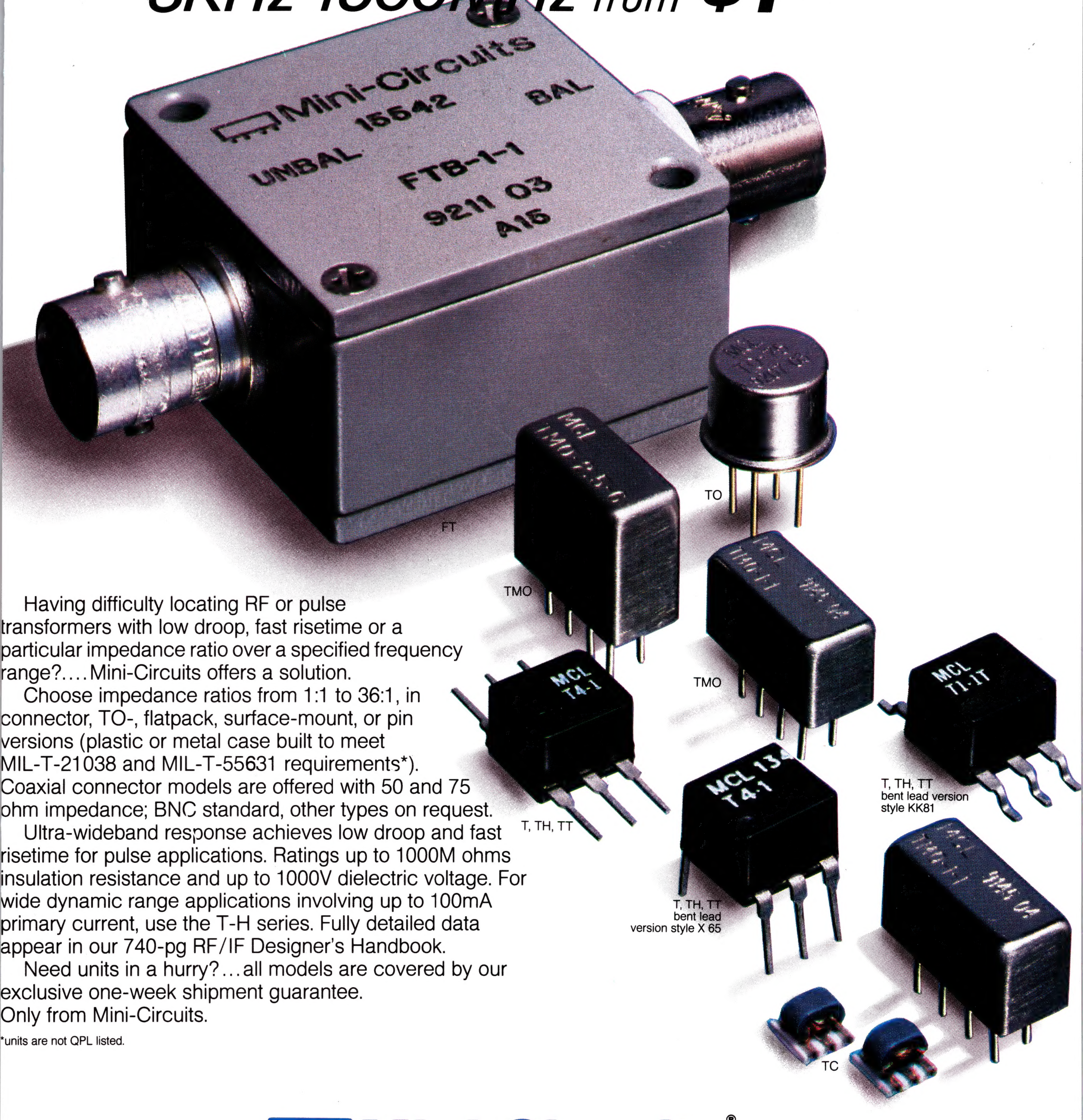

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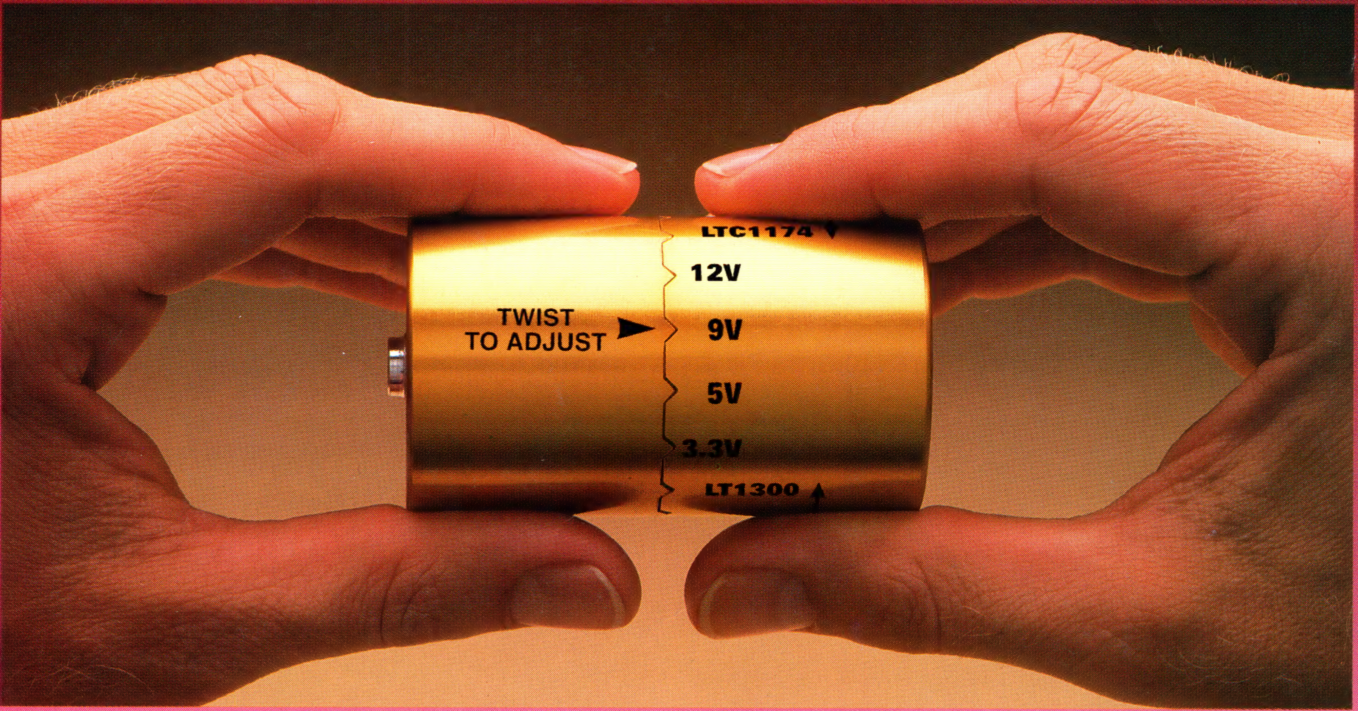

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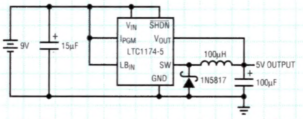

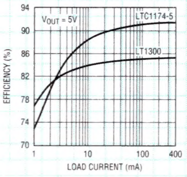

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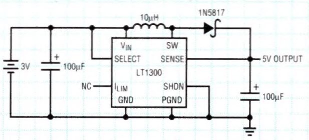

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